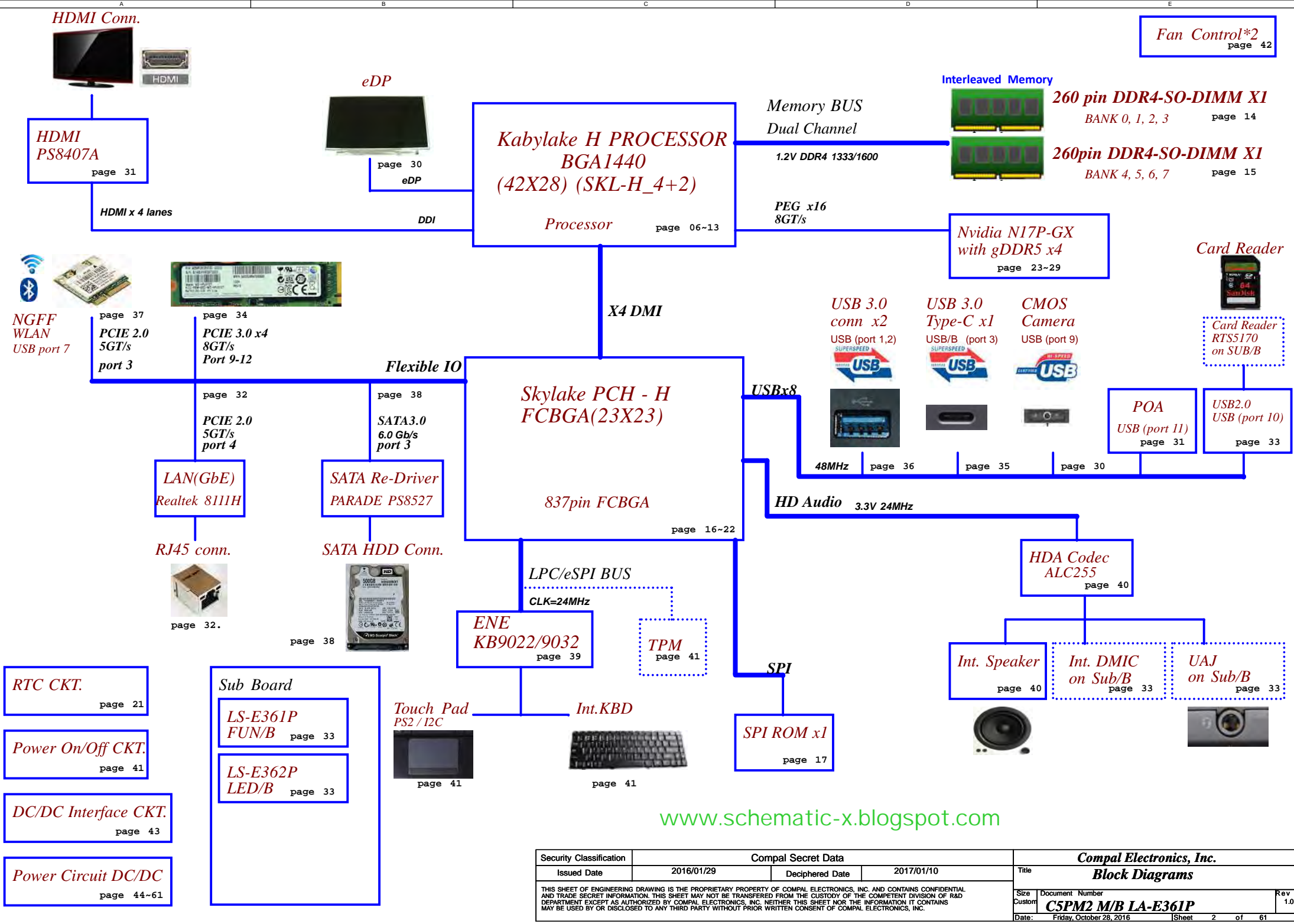


**2016.10.27**

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						C5PM2_LA-E361P		1.0			



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		C5PM2 M/B LA-E361P		1.0	
Date:		Friday, October 28, 2016		Sheet 2 of 61	

<b>Vcc</b>	<b>3.3V +/- 5%</b>				
<b>Ra</b>	<b>100K +/- 5%</b>				
<b>Board ID</b>	<b>Rb</b>	<b>V<sub>BID</sub> min</b>	<b>V<sub>BID</sub> typ</b>	<b>V<sub>BID</sub> max</b>	<b>EC AD</b>
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19	NC	3.000 V	3.000 V		0xF1 - 0xFF

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)	Touch Panel	reserved		
I2C_1 (+3VS)	TM-P2969-001 (Touch Pad)			
	SB8787-1200 (Touch Pad)			
PCH_SMBCLK (+3VS)	DIMM1			
	DIMM2			
	LIS3DHTR(G-sensor)	0x30		
PCH_SML1CLK (+3VS)	N17P-GX (VGA)	0x9E		
	EC			
EC_SMB_CK1 (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		

[illegible]

<i>SIGNAL</i>	<i>SLP_S3#</i>	<i>SLP_S4#</i>	<i>SLP_S5#</i>	<i>+VALW</i>	<i>+V</i>	<i>+VS</i>	<i>Clock</i>
<i>S0 (Full ON)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>
<i>S3 (Suspend to RAM)</i>	<i>LOW</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>
<i>S4 (Suspend to Disk)</i>	<i>LOW</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>
<i>S5 (Soft OFF)</i>	<i>LOW</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>

[illegible]

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+3VALW_PCH_PRIM	+3VALW power for PCH power rails	ON	ON	ON	ON*
+3VALW_SPI	+3VALW_PRIM supply for the SPI IO	ON	ON	ON	ON
+1.0VALW	+1.0V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.0V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+VGA_CORE	Core voltage for VGA	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+VGA_CORE_S	Core voltage for VGA				
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.					

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	



BIOS ver: V0.01  
EC: ver: V0.01

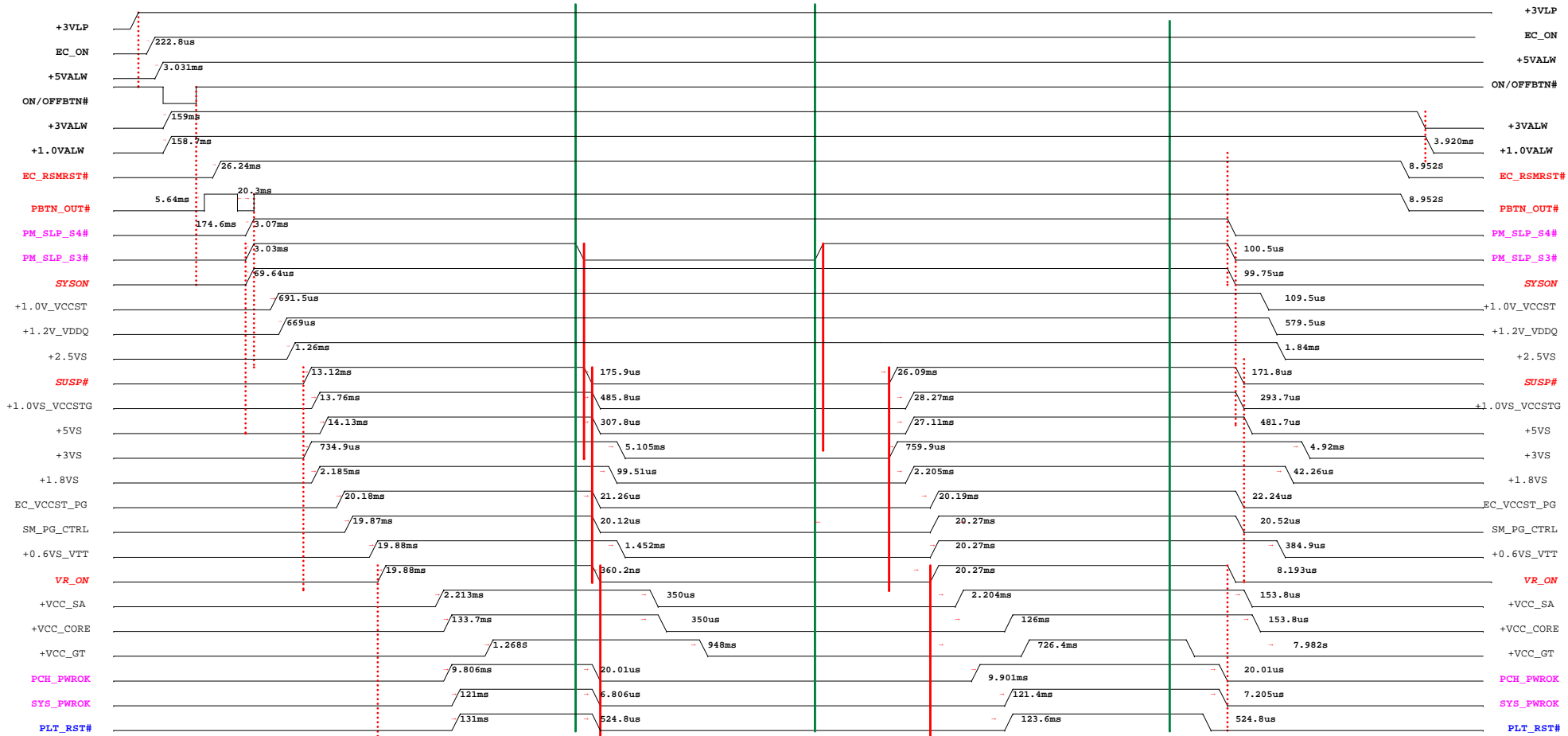
Plug in

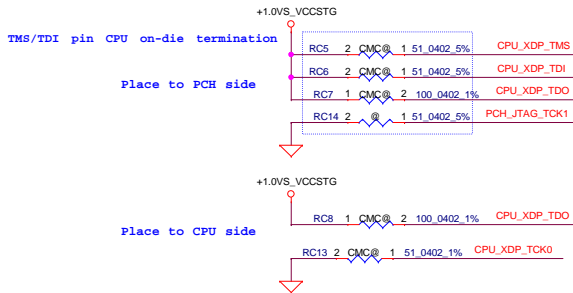
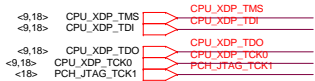
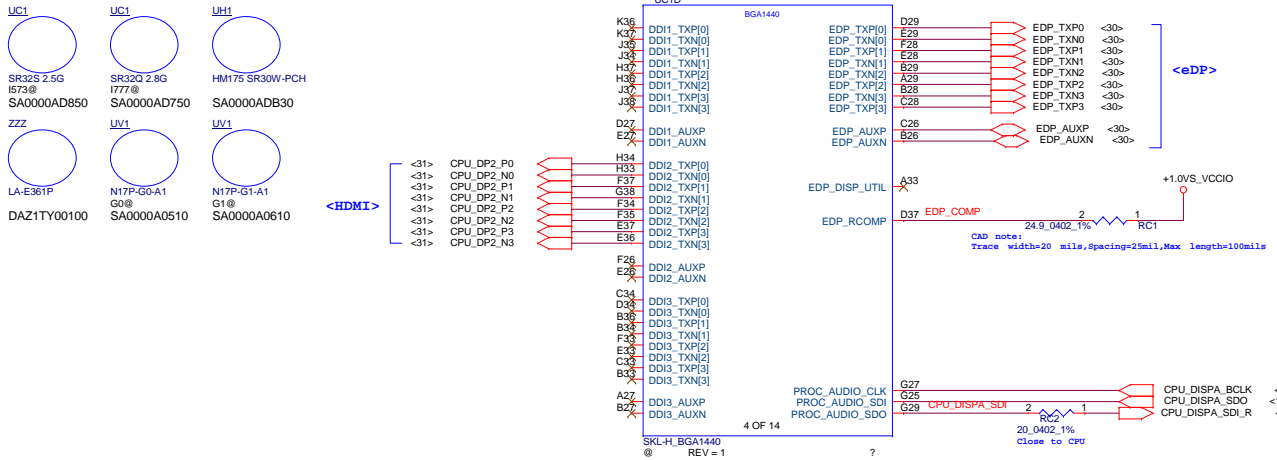
Power On

S3

S3 Resume

Power Off

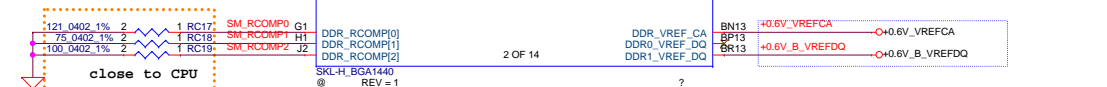
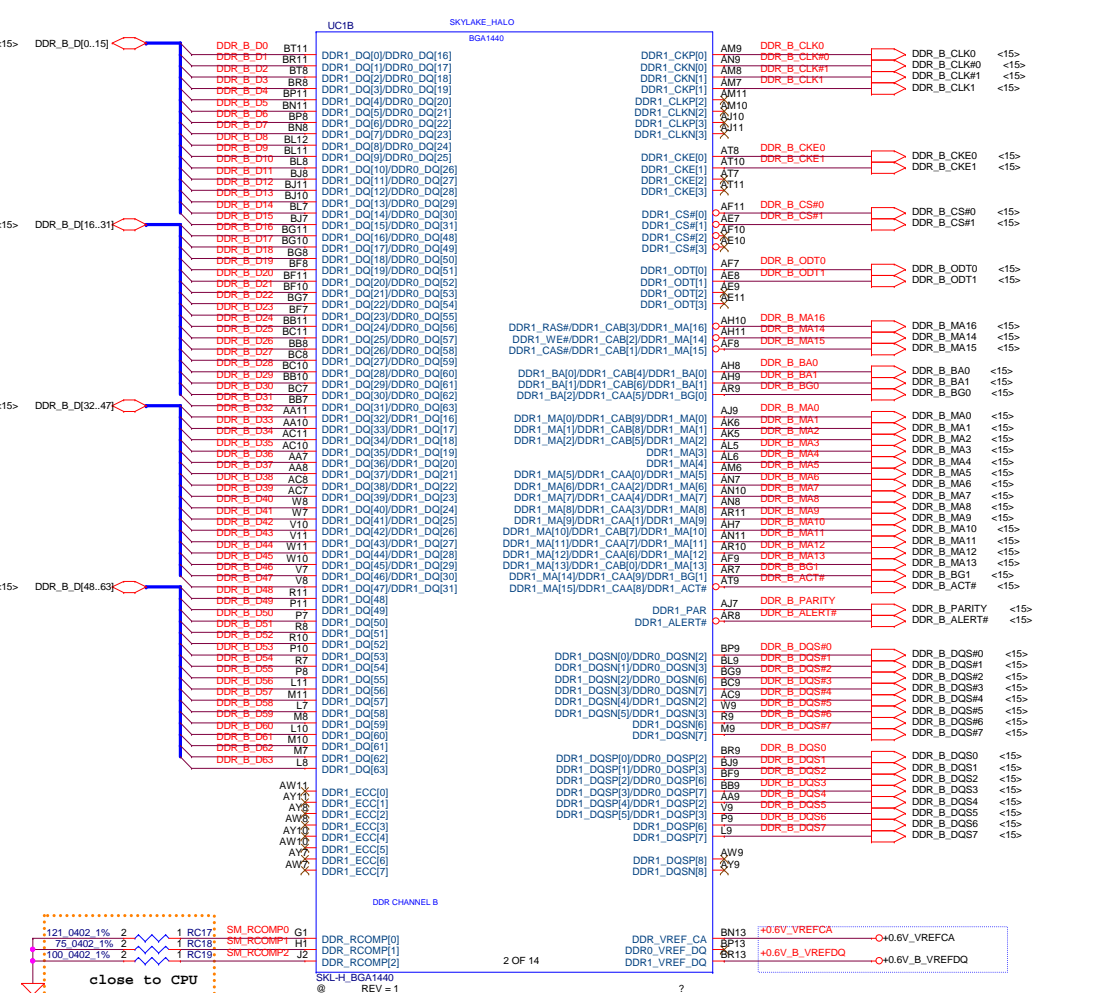
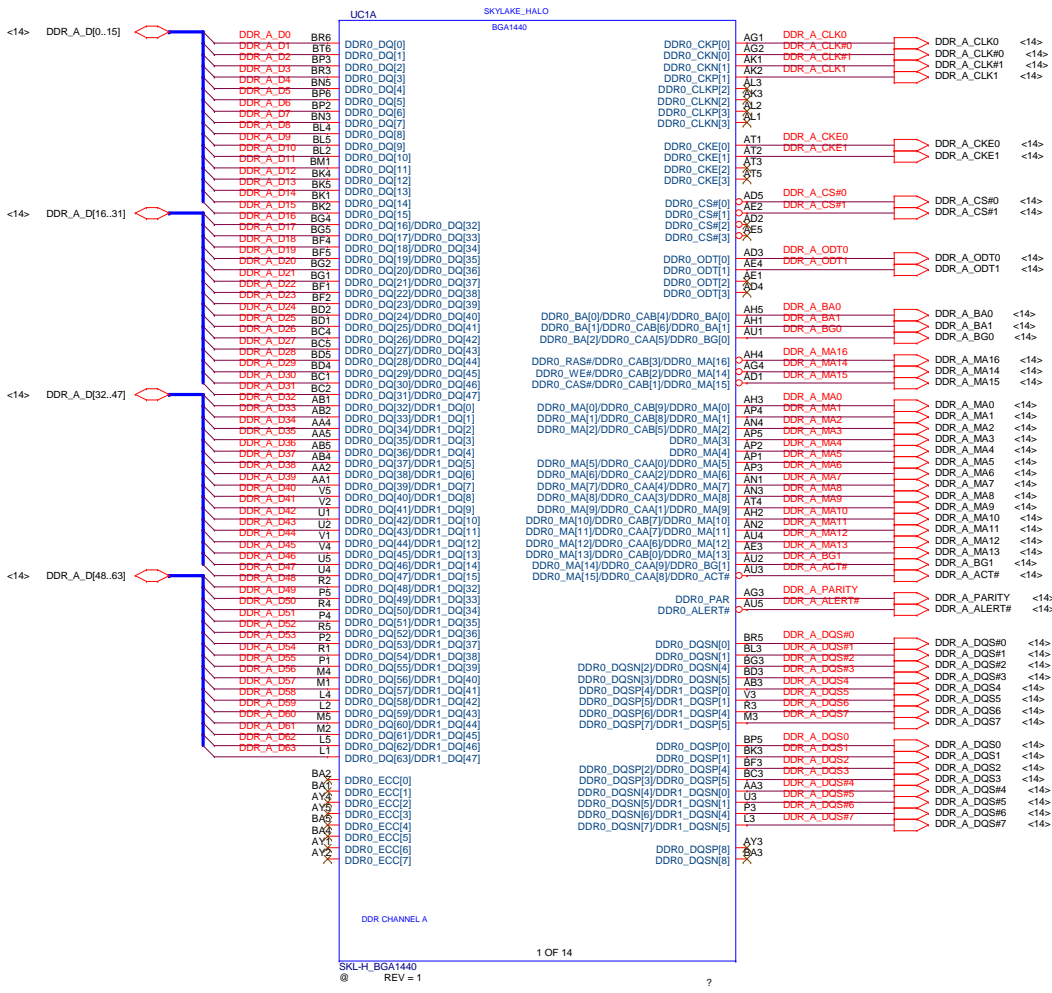




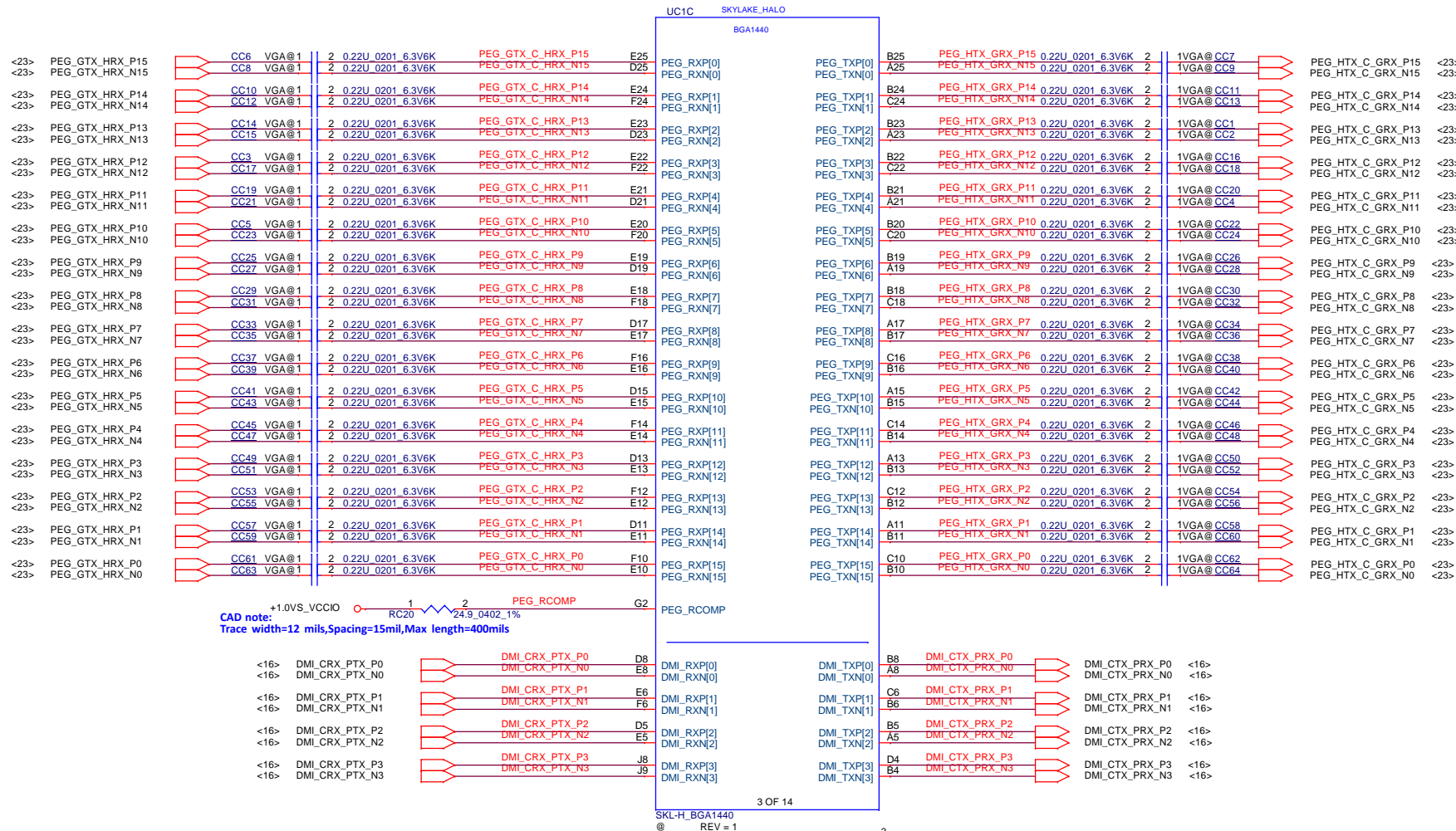
If need debug from usb port. this cmc@ need pop

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# Interleaved Memory



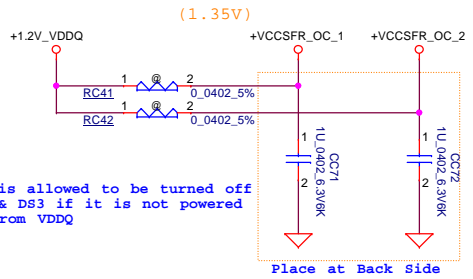
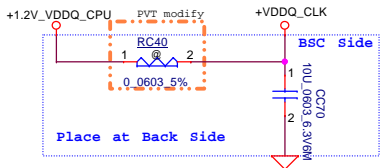
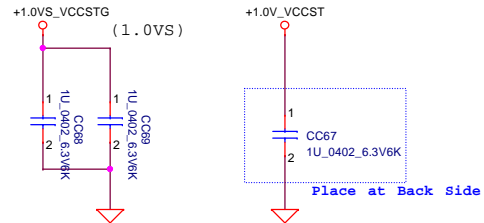
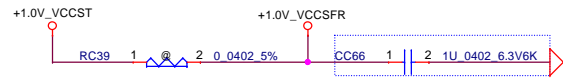




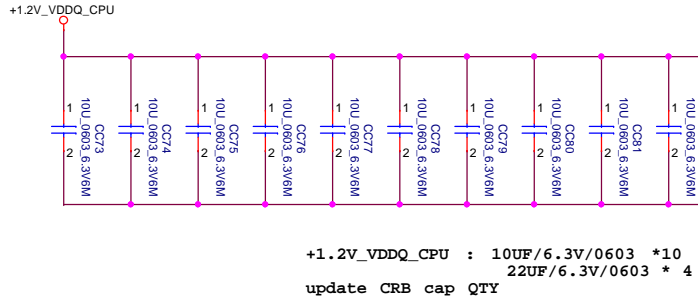








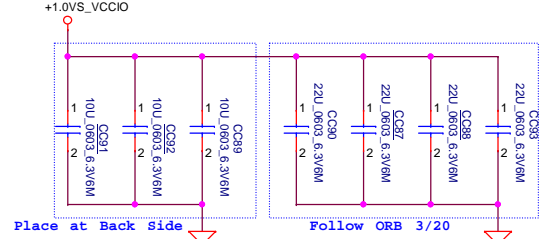
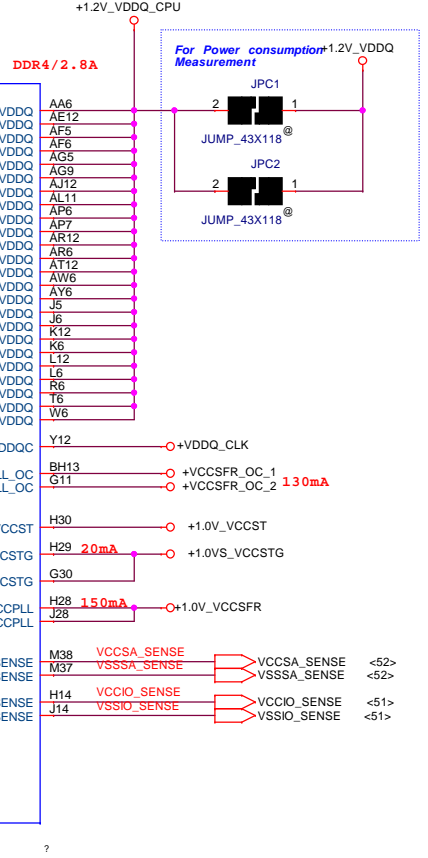
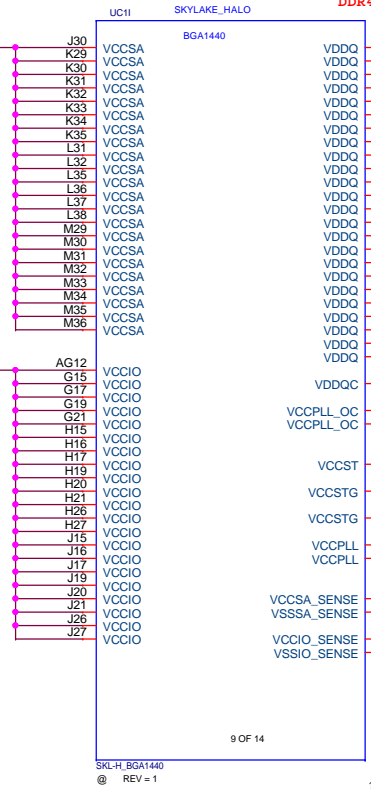
NOTE:  
VCCPLL\_OC is allowed to be turned off during S3 & DS3 if it is not powered directly from VDDQ



+1.2V\_VDDQ\_CPU : 10UF/6.3V/0603 \*10  
22UF/6.3V/0603 \* 4  
update CRB cap QTY

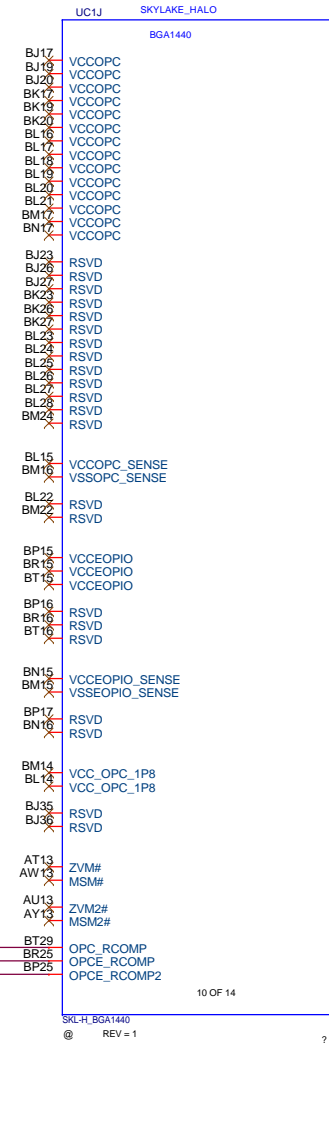
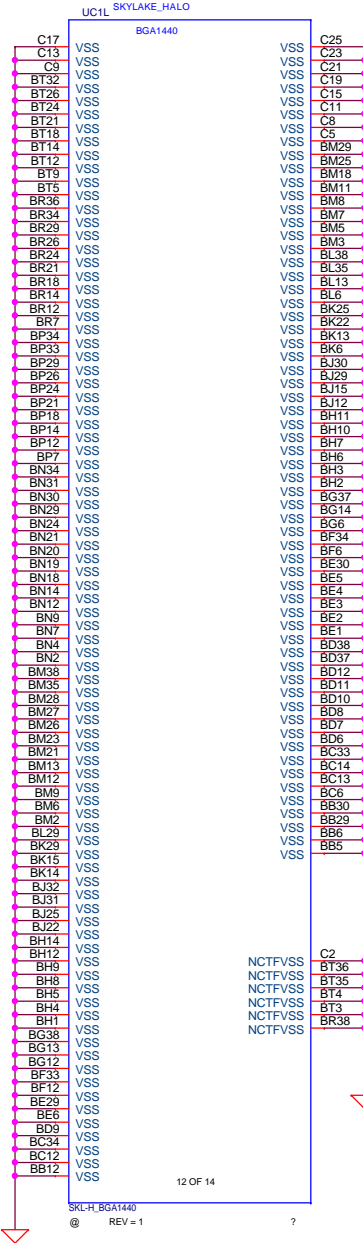
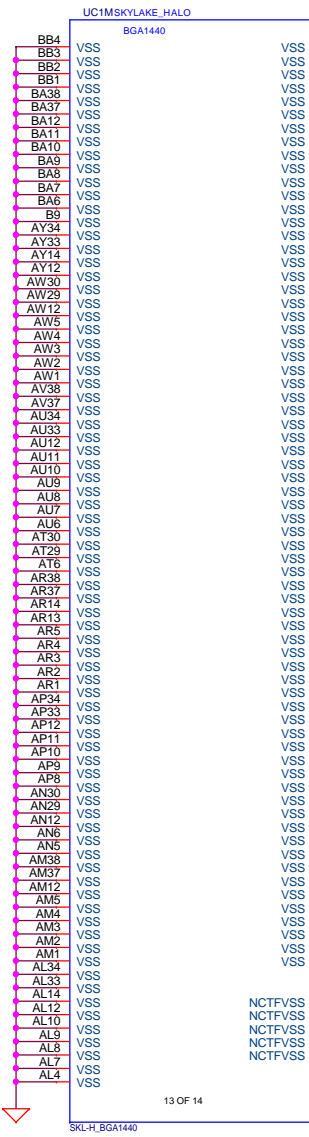
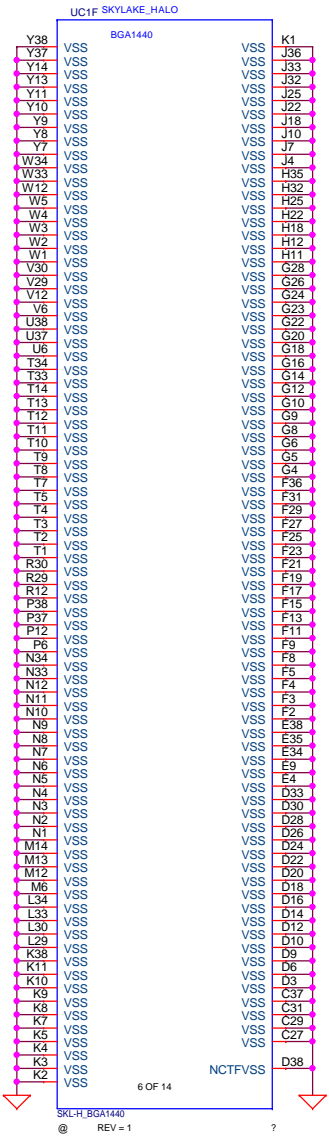
RVP11 47u\*1,10u\*7,1u\*3  
CAP place on PWR side.  
+VCC\_SA  
H-4+2/11.1A

RVP11 +1.0VS\_VCCIO  
PWR NEED PROVIDE  
0.95V FOR VCCIO  
H /5.5A

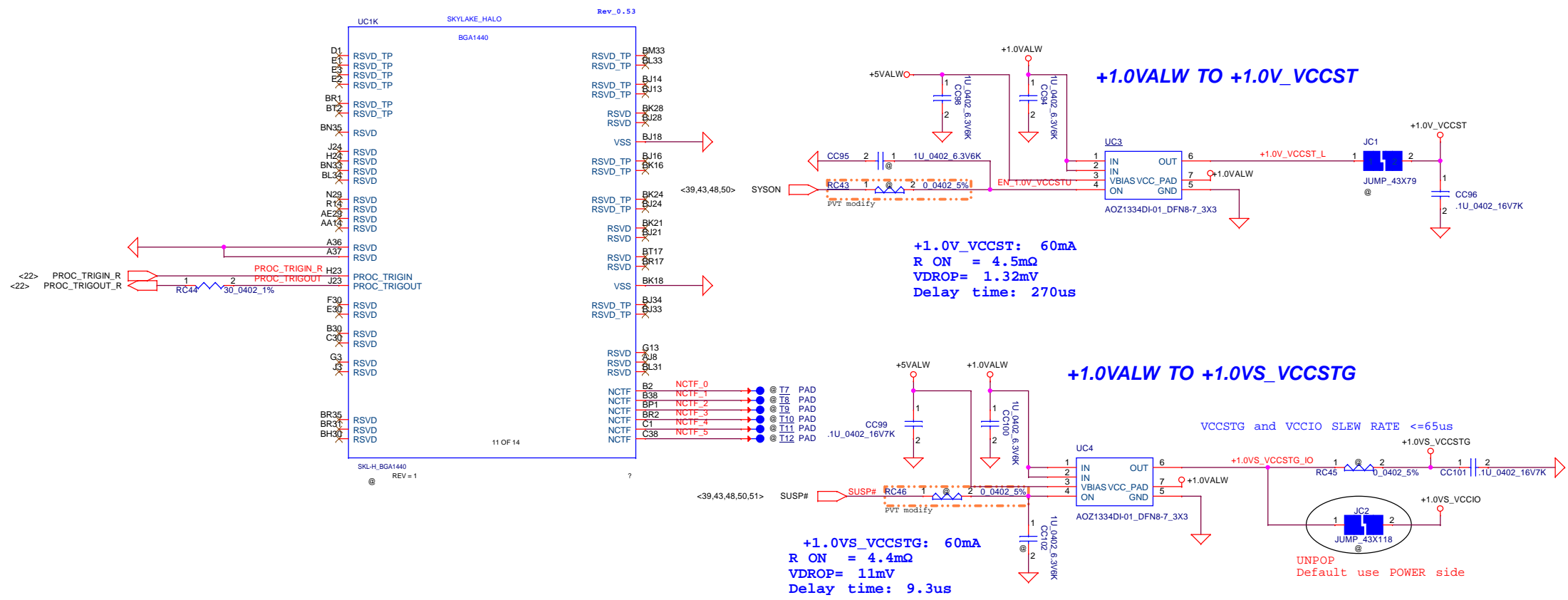


CPU\_CORE/VCCGT/VCCSA decoupling capacitor place to PWR side

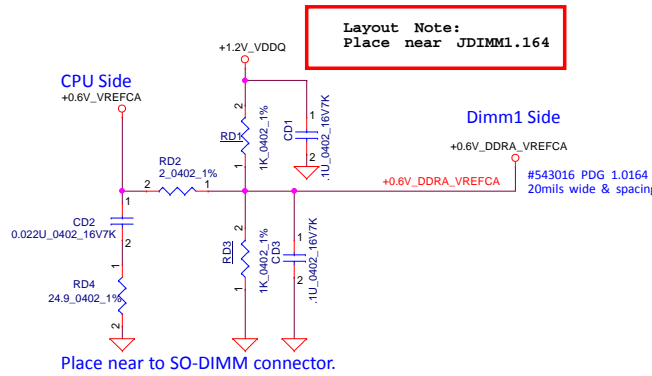
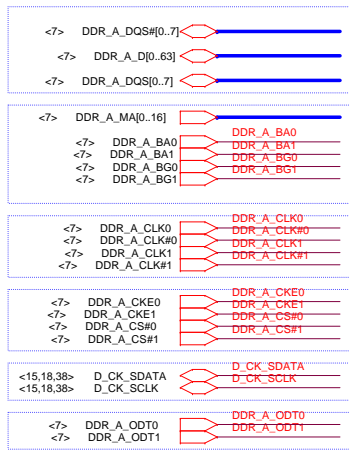
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				Date: Friday, October 28, 2016				
				Sheet 12 of 61				



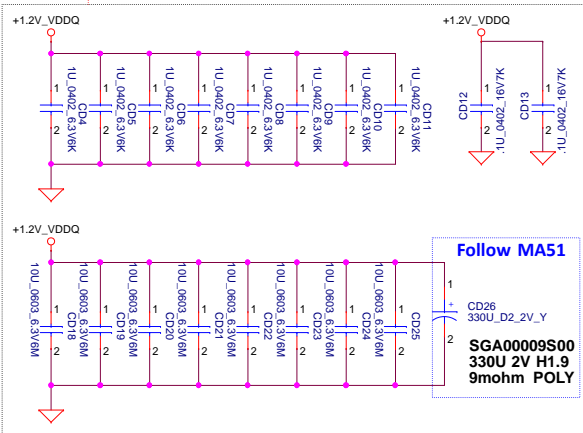
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						Date:		Friday, October 28, 2016		Sheet		13 of 61			



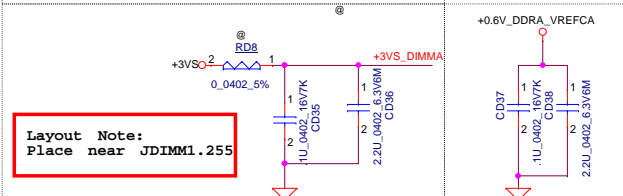
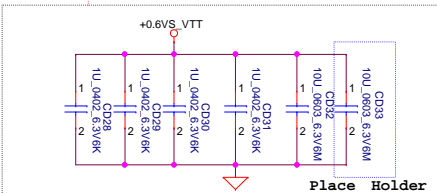
**Layout Note:**  
Place near JDIMM1

**Note:**  
place caps close to DIMM 4 on each side of DIMM

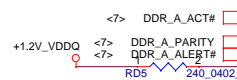
**Layout Note:**  
Place near JDIMM1.257/259



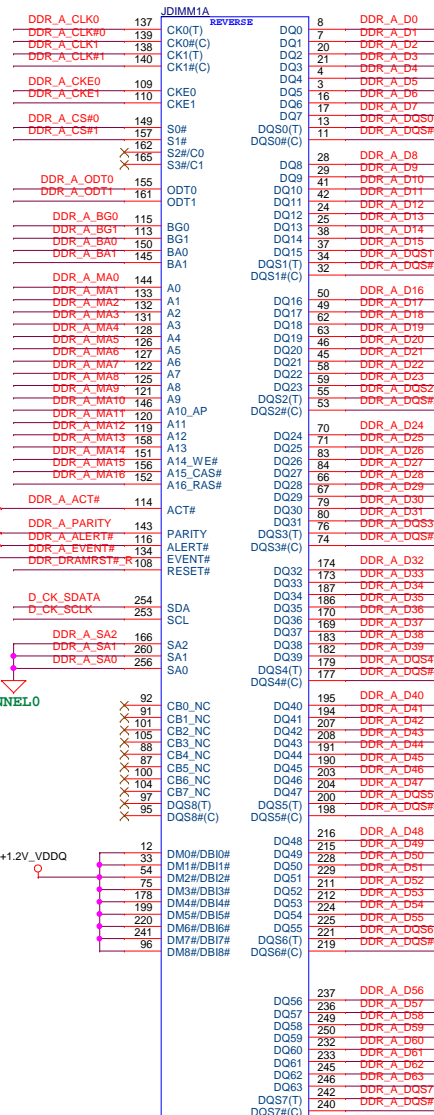
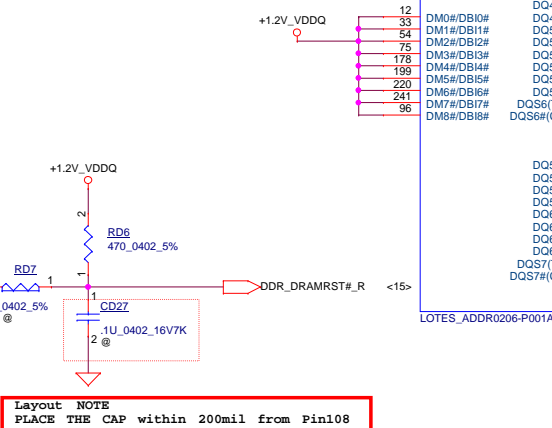
**Layout Note:**  
Place near JDIMM1.258



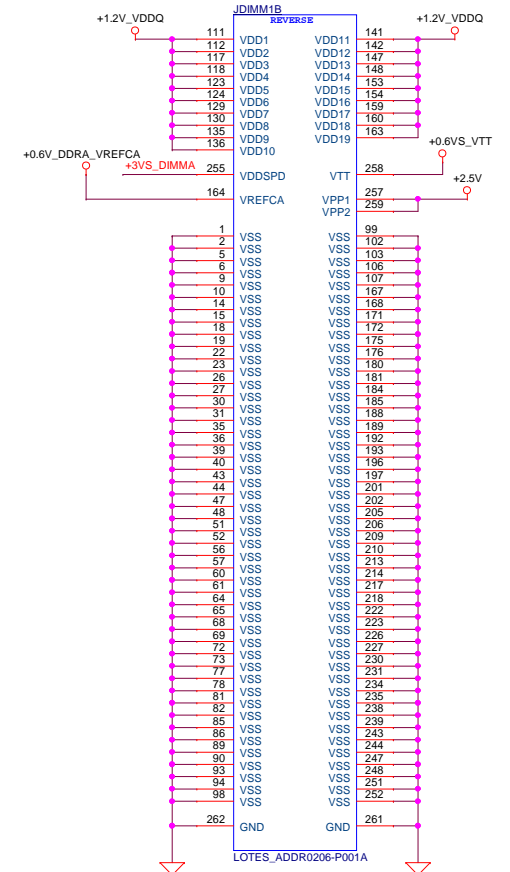
**Layout Note:**  
Place near JDIMM1.164  
within 200mils



SPD Address for CHANNEL0  
Write Address 0xA0  
Read Address 0xA1  
SA0=0;SA1=0;SA2=0



**Reverse Type-4H**  
2-3A to 1 DIMMs/channel



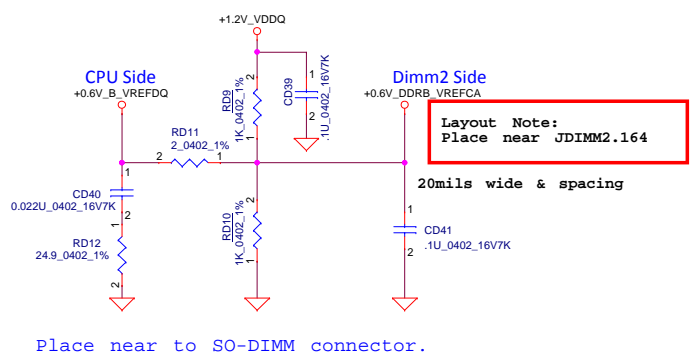
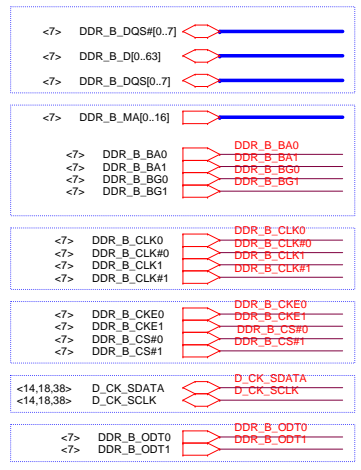
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					Size	Document	Number	<b>C5PM2 M/B LA-E361P</b>		Rev		
					Custm					1.0		
					Date:	Friday, October 28, 2016	[Sheet			14	of	61



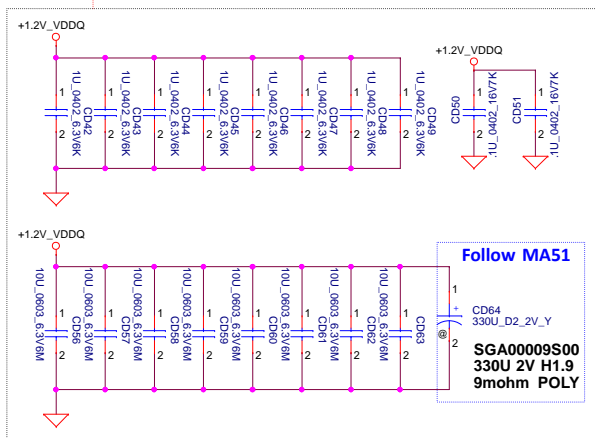
# Reverse Type-8H

## 2-3A to 1 DIMMs/channel

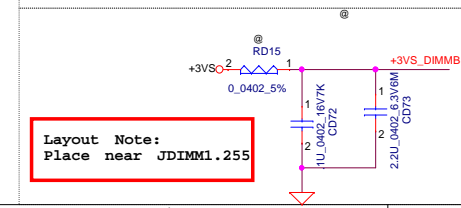
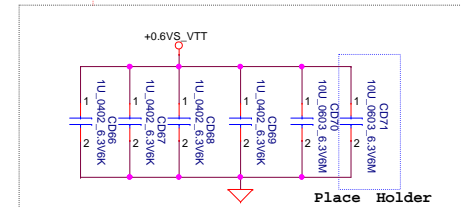


**Layout Note:**  
Place near JDIMM2

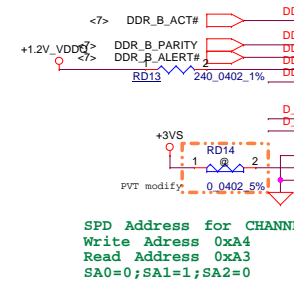
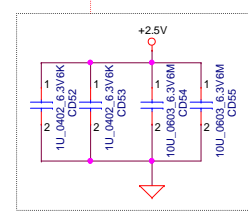
**Note:**  
place caps close to DIMM 4 on each side of DIMM



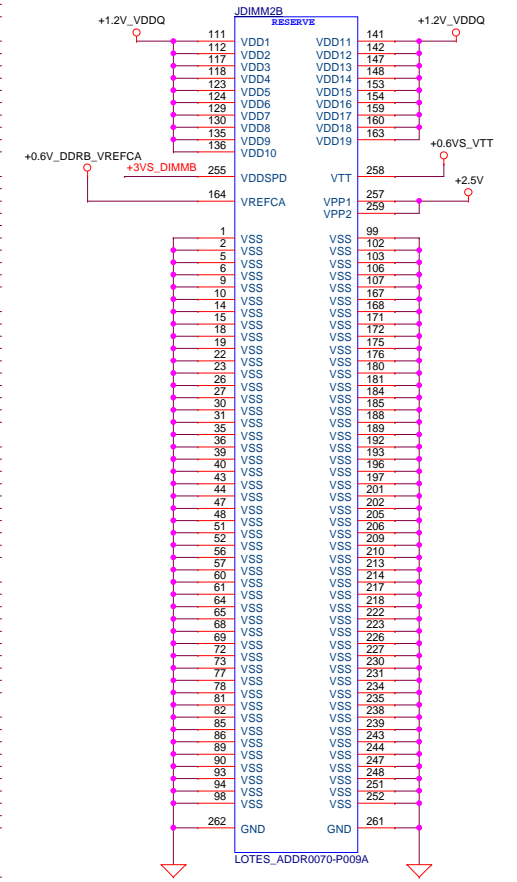
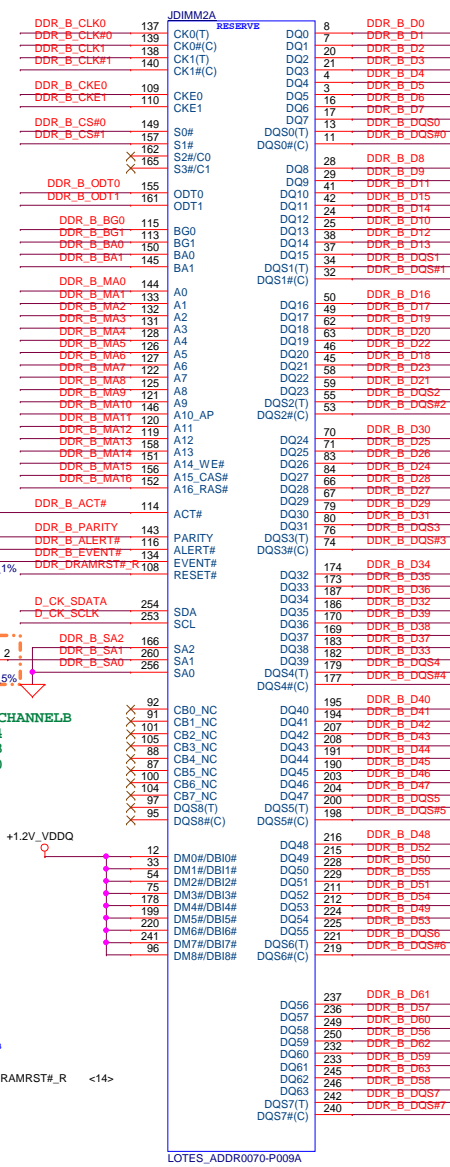
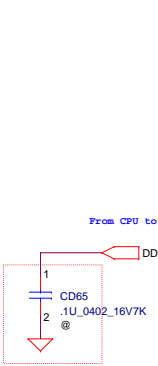
**Layout Note:**  
Place near JDIMM2.258



**Layout Note:**  
Place near JDIMM2.257/259

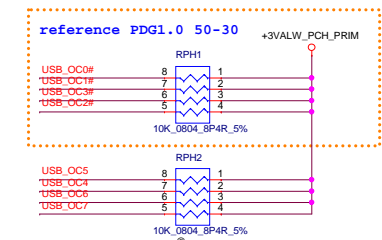
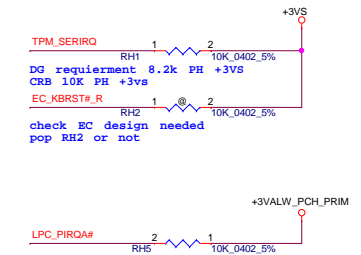


**SPD Address for CHANNELB**  
Write Address 0xA4  
Read Address 0xA3  
SA0=0;SA1=1;SA2=0



# Interleaved Memory



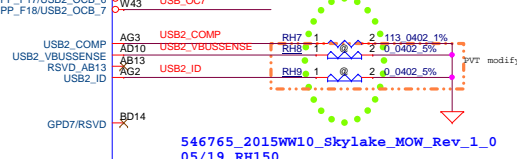


CHECK ACER DVR for port use  
12/08 Change Port, follow DVR1044\_R1.03

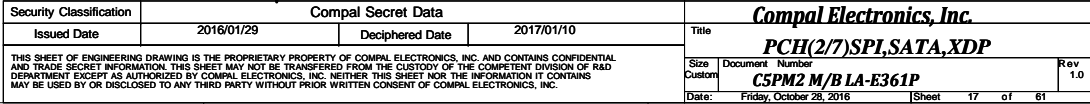
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D16	PCIe5_TXN
C27	PCIe5_TXP
G27	PCIe6_RXN
E27	PCIe6_RXP
B27	PCIe6_TXN
A27	PCIe6_TXP
L27	PCIe7_RXN
K27	PCIe7_RXP
C28	PCIe7_TXN
B28	PCIe7_TXP
K28	PCIe8_RXN
L28	PCIe8_RXP
C28	PCIe8_TXN
B28	PCIe8_TXP

SKL-H-PCH\_BGA837  
REV = 1.3

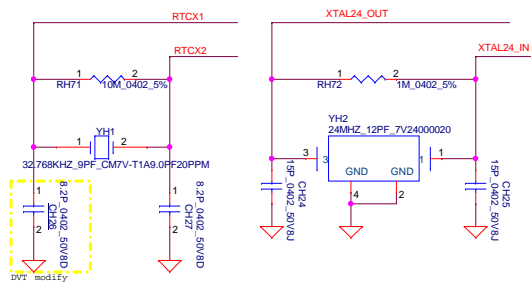
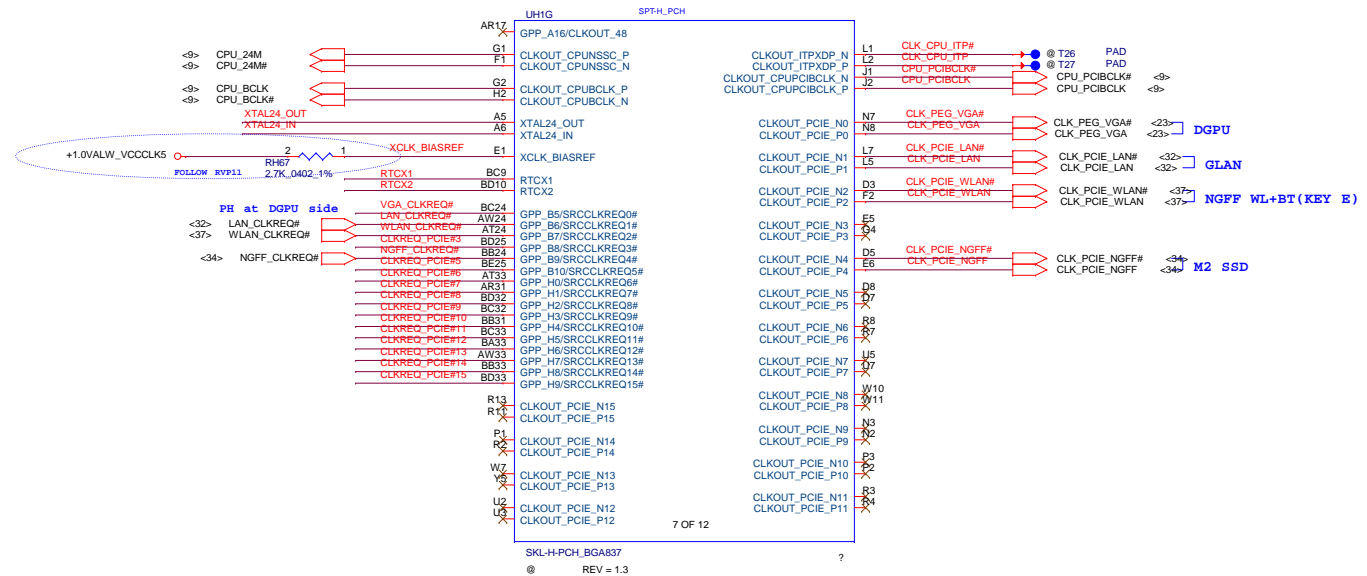
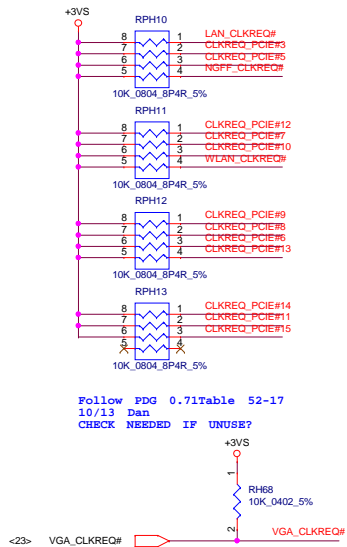
2 OF 12



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		Size Custom		Document Number		C5PM2 M/B LA-E361P			Rev 1.0	
		Date		Friday, October 26, 2016						
						Sheet 16 of 61				





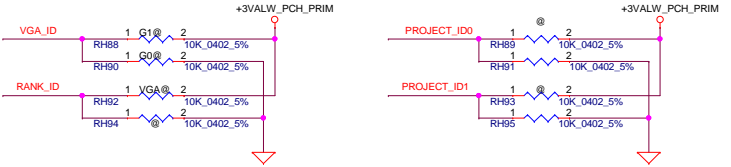
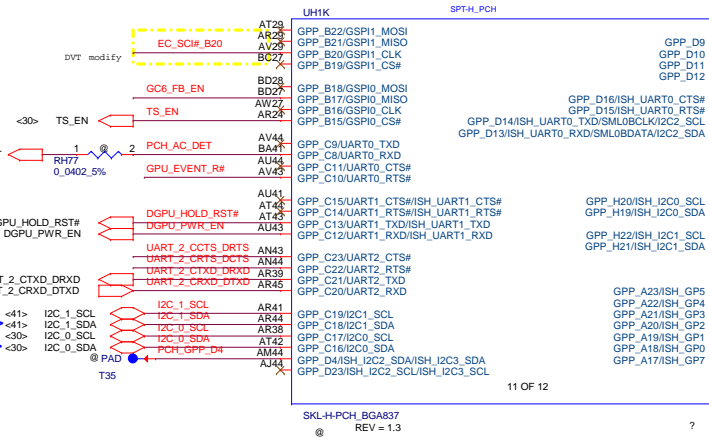


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Date:	Friday, October 28, 2016	Sheet	19	of	61

```

GSP1_MOSI / GPP_B22
int. PD
Boot BIOS Destination
0 = SPI (Default)
1 = LPC
.....
SPI0_MOSI / GPP_B18
int. PD
= Disable " No Reboot " mode ( Default )
= Enable " No Reboot " mode ( Programmable timer system reboot feature).

```

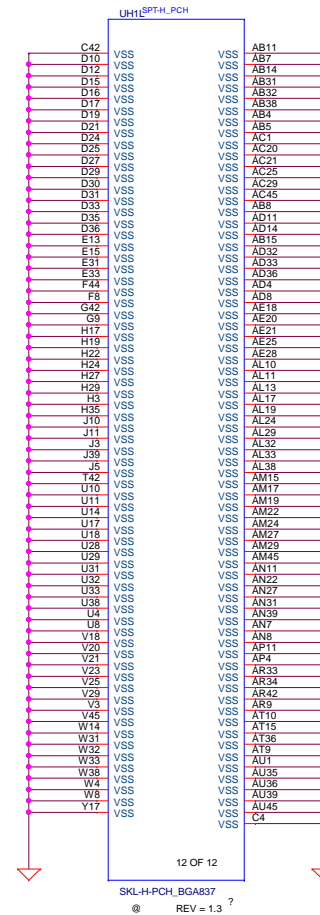
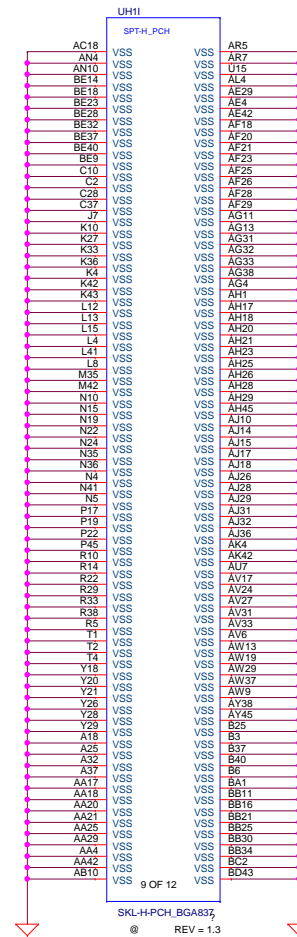
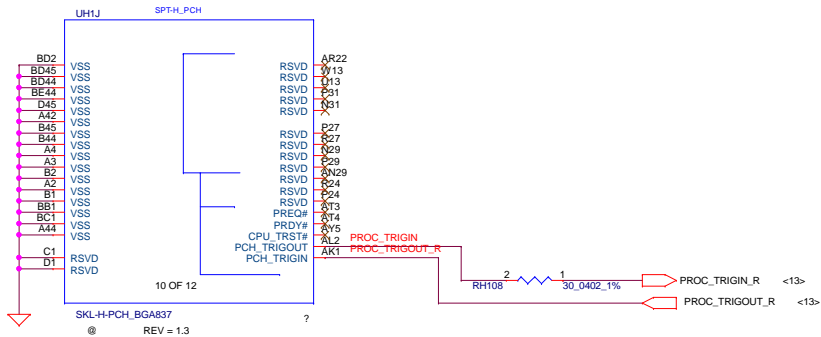


RANK_ID	GPP_D10
DR	0
SR	1

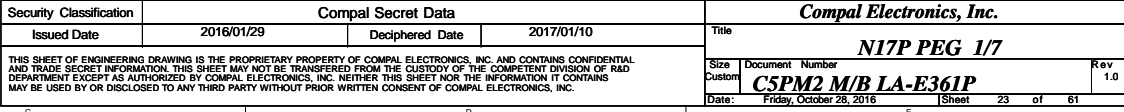
Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
* C5PM2	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1



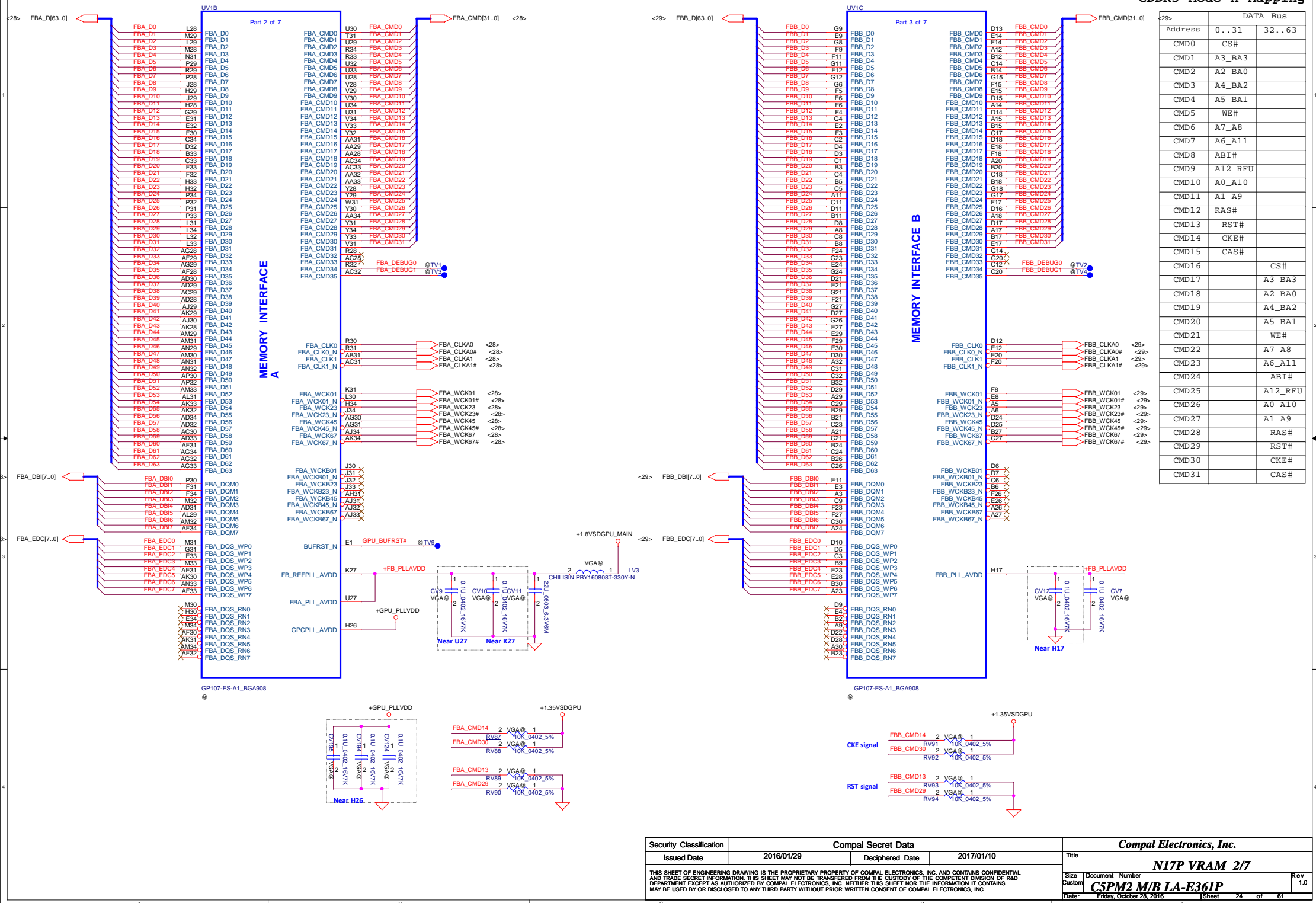


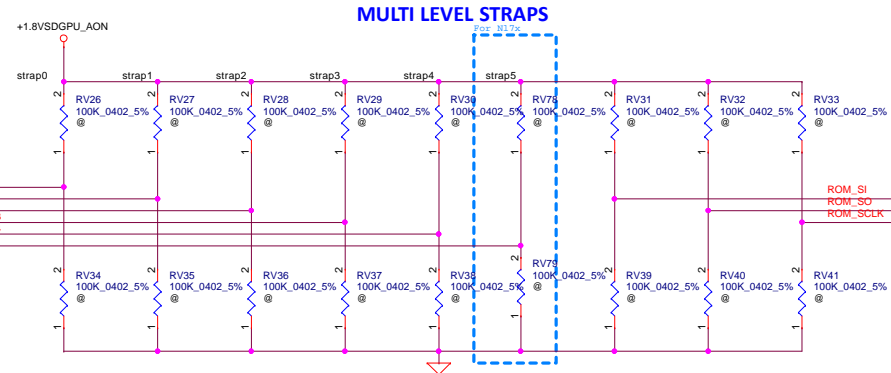
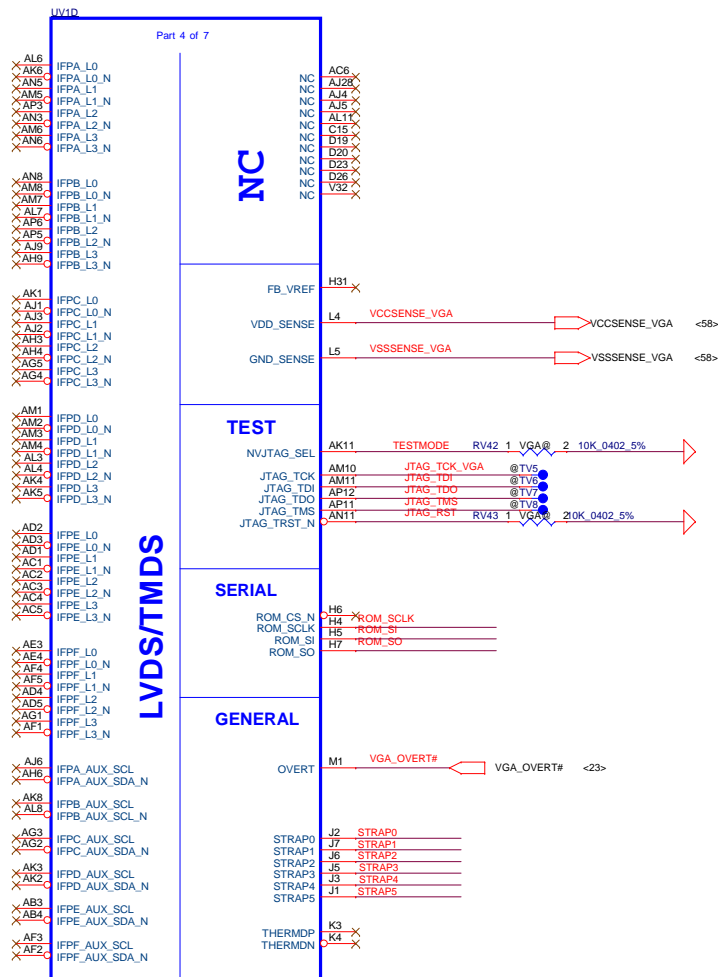






# GDDR5 Mode H Mapping





Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V <sup>2</sup>	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production candidate
4 Gb	128Mx32	1.35V and 1.5V <sup>2</sup>	Samsung	K4G41325FE-HC28	E-die	0x7	7 Gbps	N/A	Full	Production candidate
			Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production candidate
			Micron	EDW4032BABG-70:F	A-die	0x8	7 Gbps	N/A	Full	Post production candidate

Table 5.2 RAMCFG

Strap Pins	Strap Pins	Strap Pins	RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5.4 SORx\_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins <small>see Note</small>			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

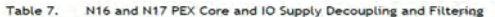
GP107-ES-A1\_BGA908

Strap Pins	Strap Pins	Strap Pins	Functions Selected by This Strapping	Functions Selected by This Strapping	Functions Selected by This Strapping	Functions Selected by This Strapping
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

SMB_ALT_ADDR	
Low	Single GPU
High	Dual GPU
DEVID_SEL	
Low	Orig. Device ID
High	Support G-Sync GPUID
VGA_DEVICE	
Low	3D Device
High	VGA Device
PCIE_CFG	
Low	Normal signal swing
High	Reduce the signal amplitude

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Size	Document	Number	Rev	1.0
Custom	CSPM2 M/B LA-E361P		Date:	Friday, October 28, 2016
Sheet	25	of	61	

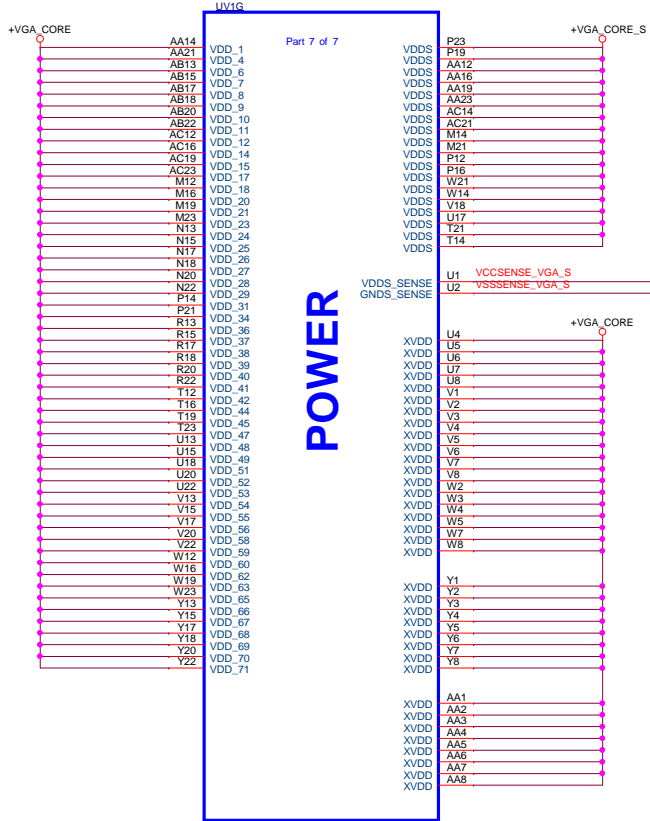




GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
<b>N16 PEX_I/OVDD (N17 PEX_DVDD) Supply Rail</b>						
GB48-128, GB4C-128	1.0 $\mu$ F	X65	0402	2	4	Under GPU
	4.7 $\mu$ F	X65	0603	1	2	Floor GPU
	10 $\mu$ F	X5R	0805	2	2	Midway between GPU and Power Supply
	22 $\mu$ F	X5R	0805	2	1	Midway between GPU and Power Supply
<b>N16 PEX_I/OVDDQ (N17 PEX_HVDD) Supply Rail</b>						
GB48-128, GB4C-128	1.0 $\mu$ F	X65	0402	2	4	Under GPU
	4.7 $\mu$ F	X65	0603	1	2	Floor GPU
	10 $\mu$ F	X5R	0805	2	2	Midway between GPU and Power Supply
	22 $\mu$ F	X5R	0805	2	1	Midway between GPU and Power Supply

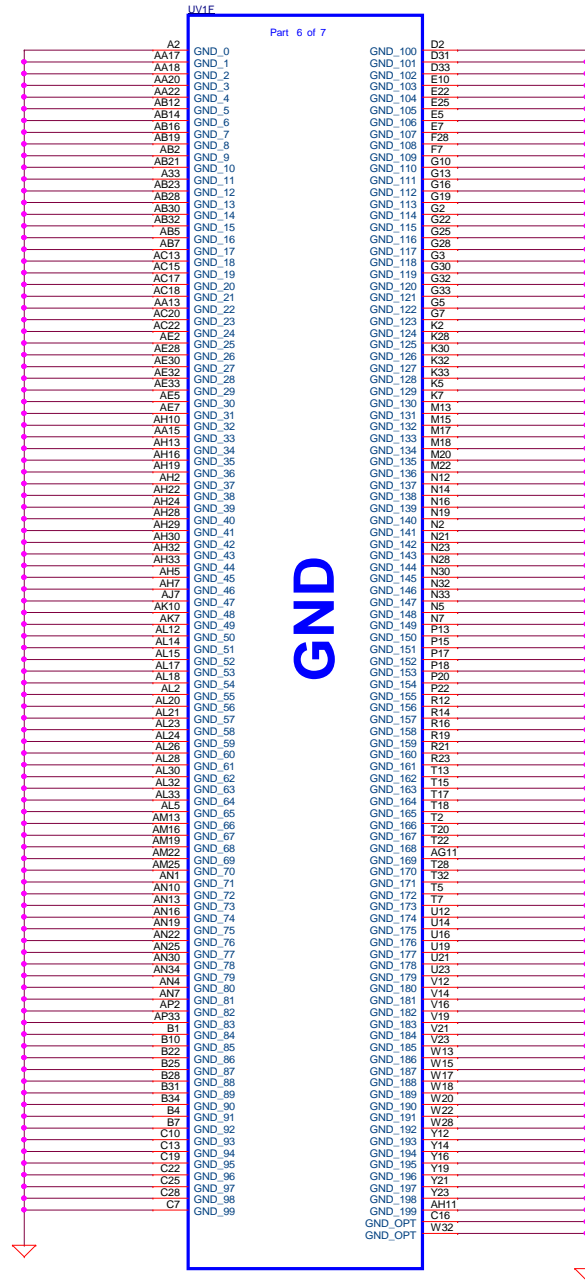
1.0 uF	X65 [0402]	12	Under GPU FBVDD0 ball
10 uF	X65 [0603]	4	
10 uF	X65 [0603]	2	Near GPU device
22 uF	X65 [0603]	5	

N17P VDD5  
1uF\*5/4.7uF\*5 (under GPU)  
330uF\*1/22uF\*3/10uF\*2/4.7uF\*2



GP107-ES-A1\_BGA908

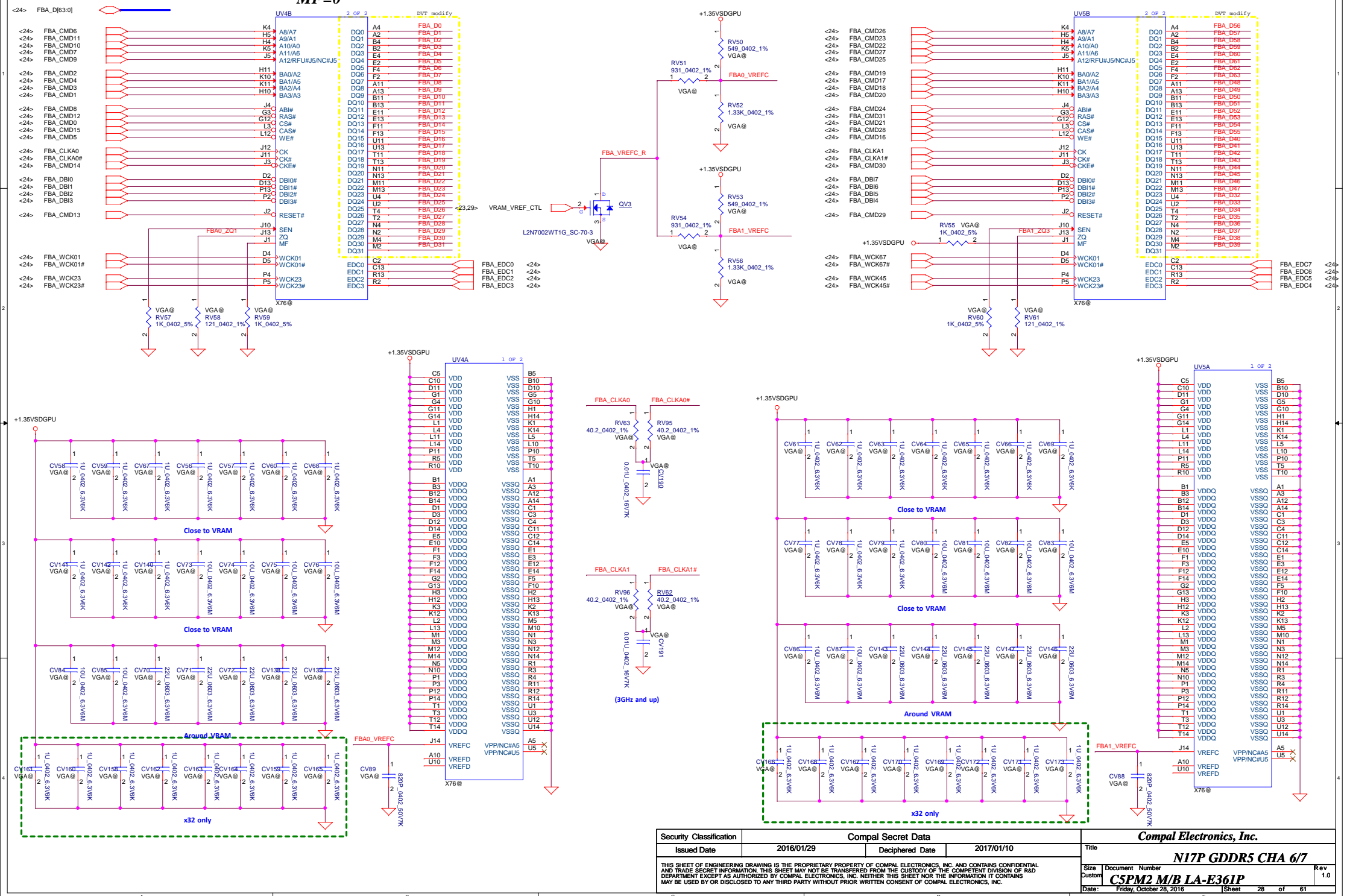
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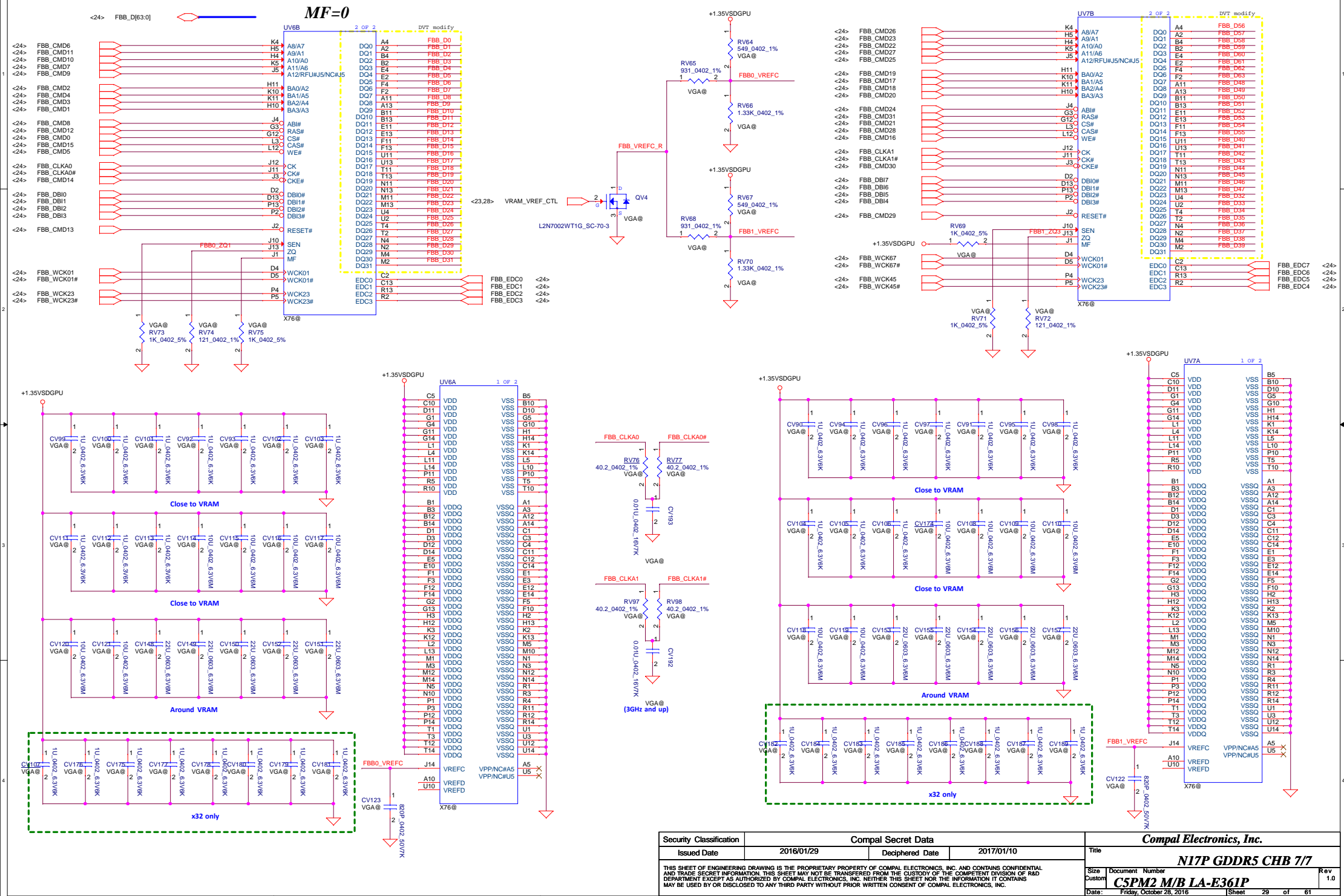


GP107-ES-A1\_BGA908

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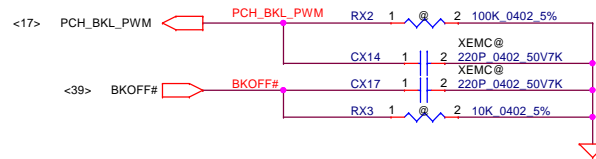
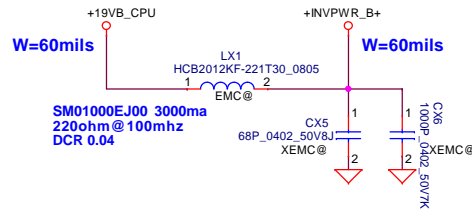
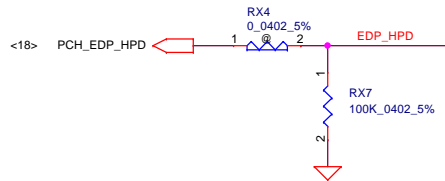
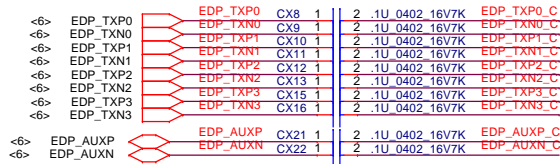
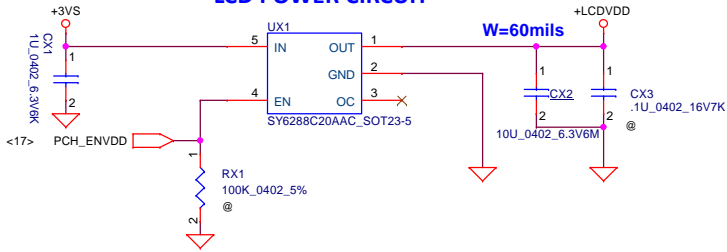
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								Size	
Customer		C5PM2 M/B LA-E361P						1.0	
Date:		Friday, October 28, 2016			Sheet		27 of 61		

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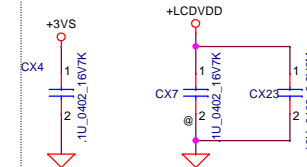




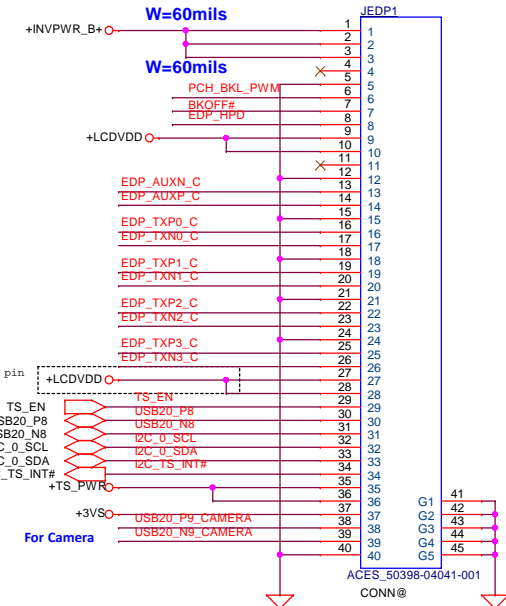
## LCD POWER CIRCUIT



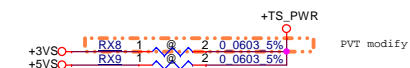
## Place closed to JEDP1



## LED PANEL Conn.



## I2C Touch Screen



SPI touch RST follow CRB #544669 P.8

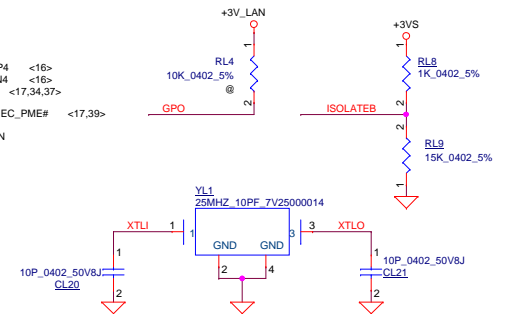
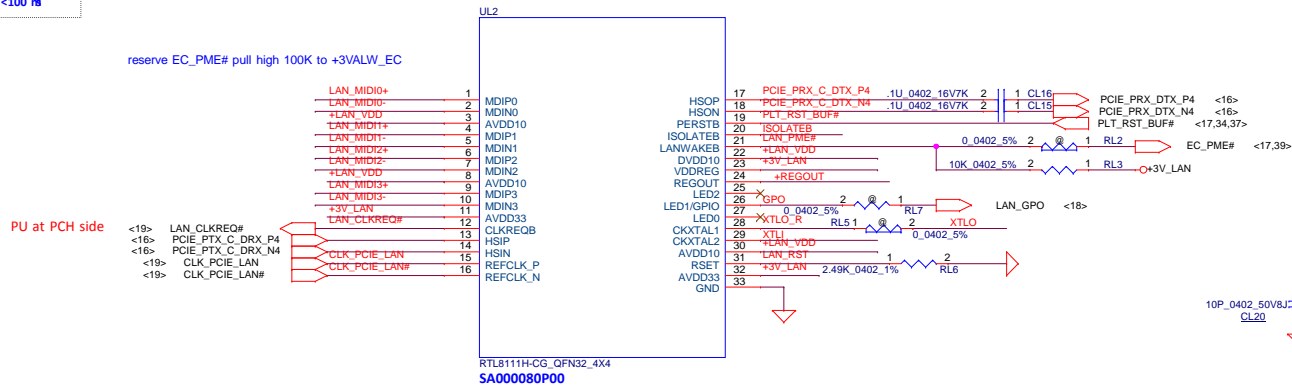
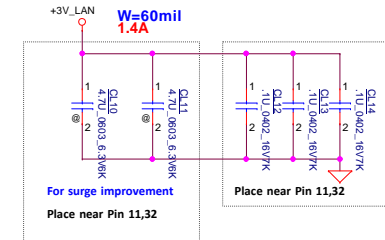
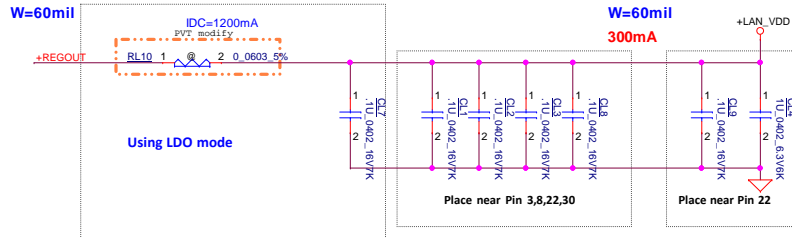
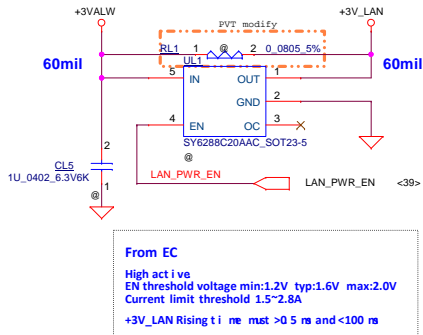
## Camera



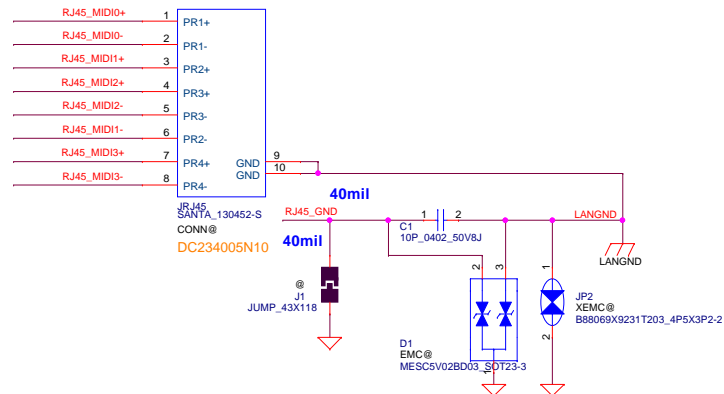
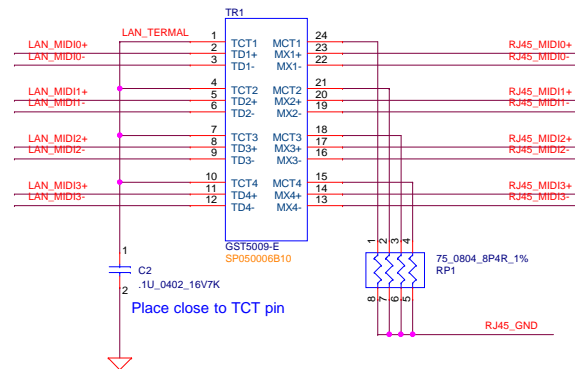
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						Size		Document Number		Rev	
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						Date:		Friday, October 28, 2016		Sheet 30 of 61	



# LAN-RTL8111H

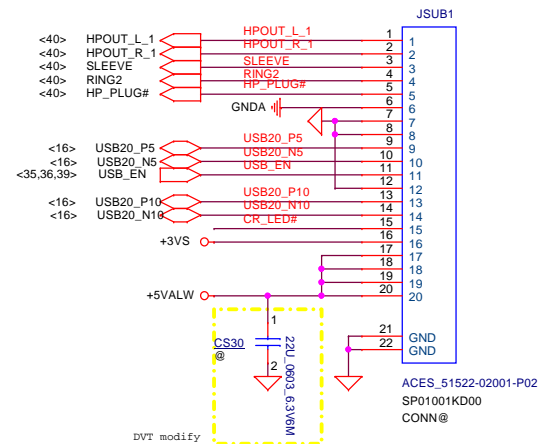


## LAN Connector

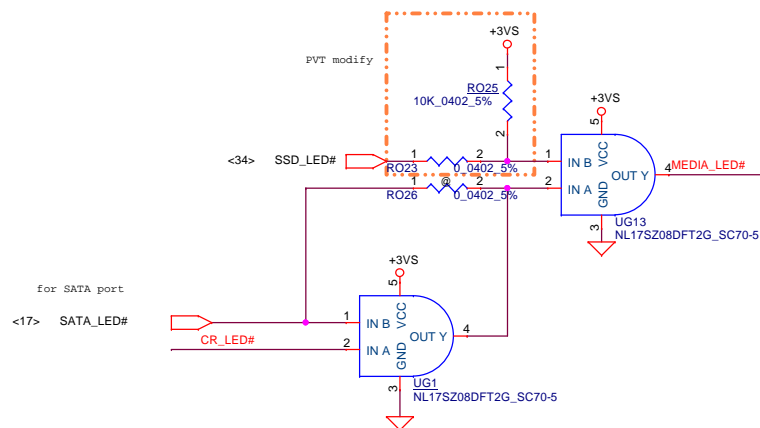
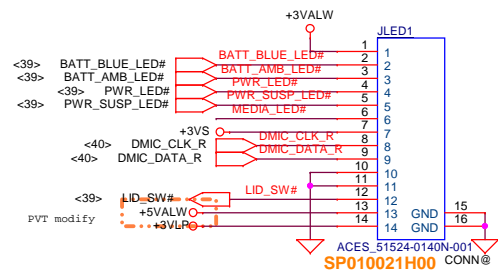


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				Date:	Friday, October 28, 2016	Sheet 32 of 61

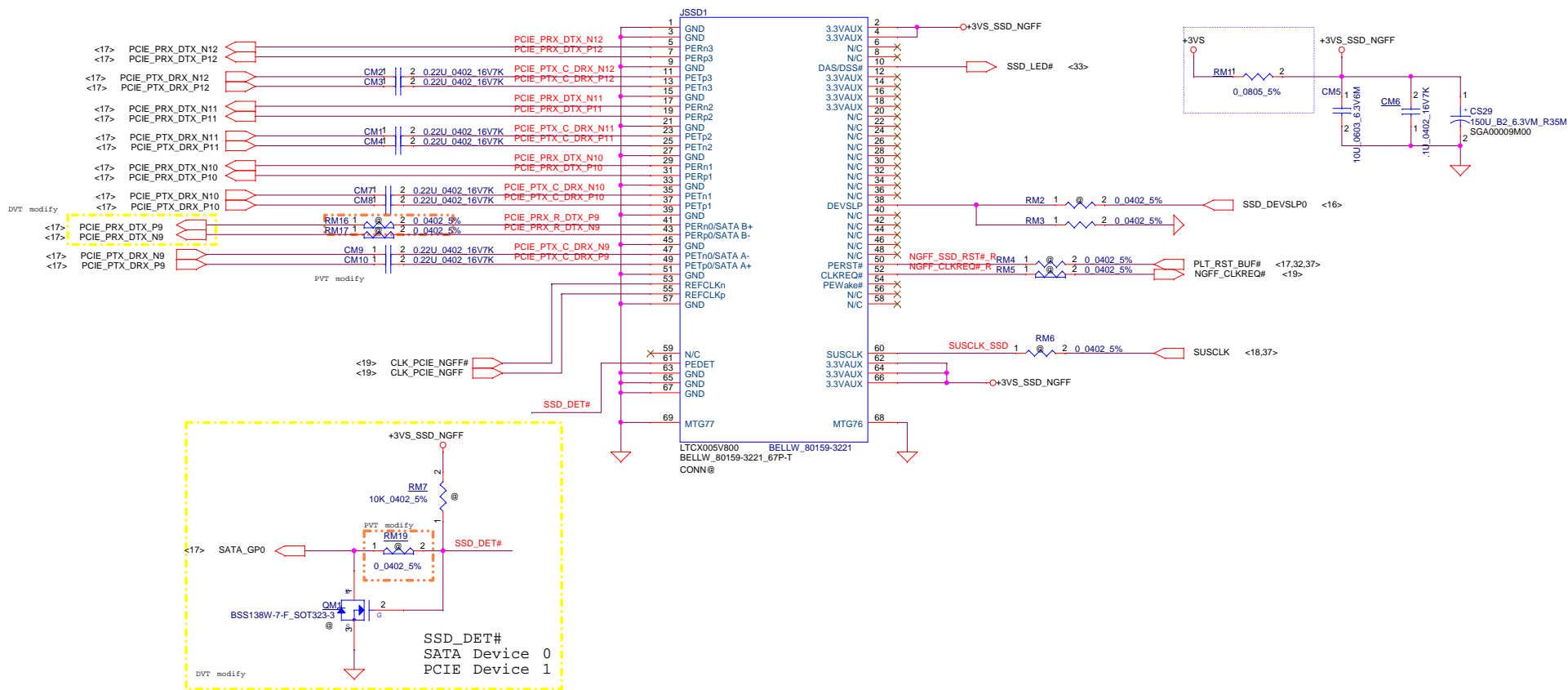
## To Fun/B (USB Port 5, + AUDIO)



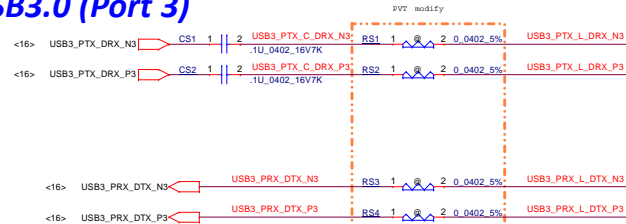
## To LED/B



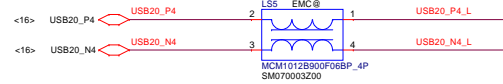
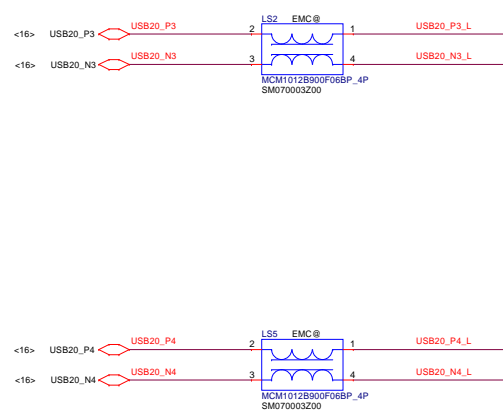
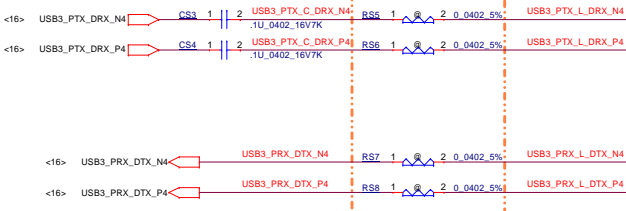
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								Size Custom	Document Number			Rev 1.0		
								C5PM2 M/B LA-E361P						
								Date:		Friday, October 28, 2016		Sheet 33 of 61		



## USB3.0 (Port 3)



## USB3.0 (Port 4)



For ESD request

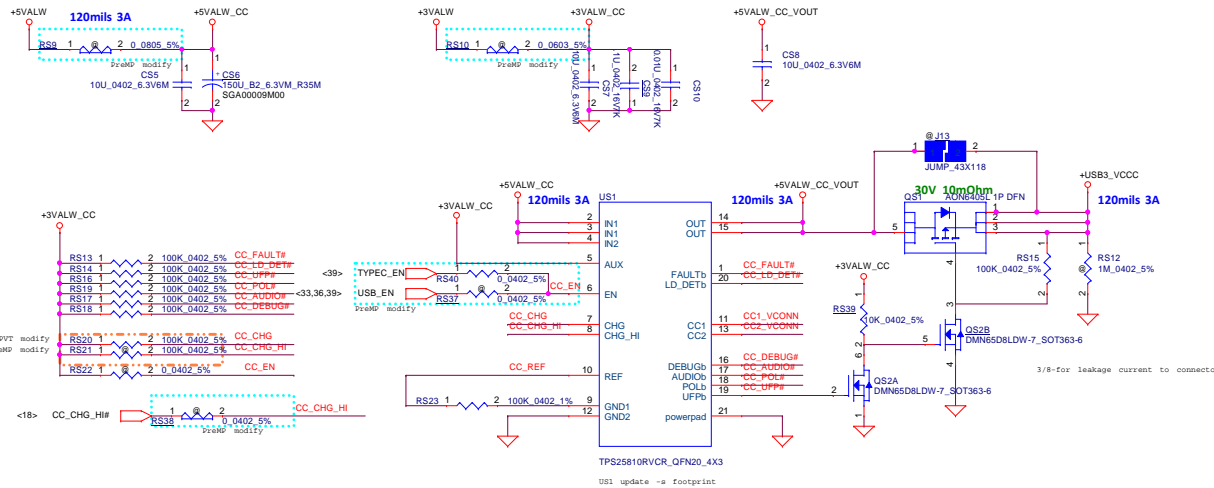
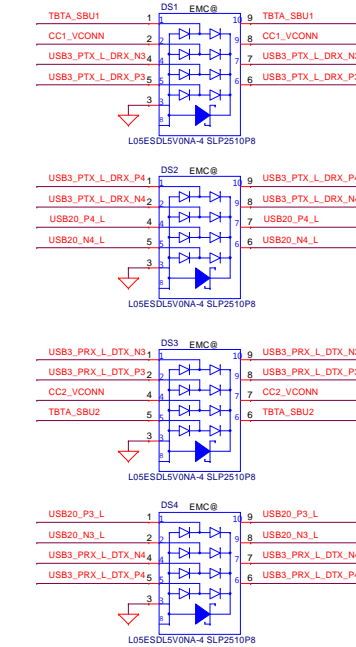
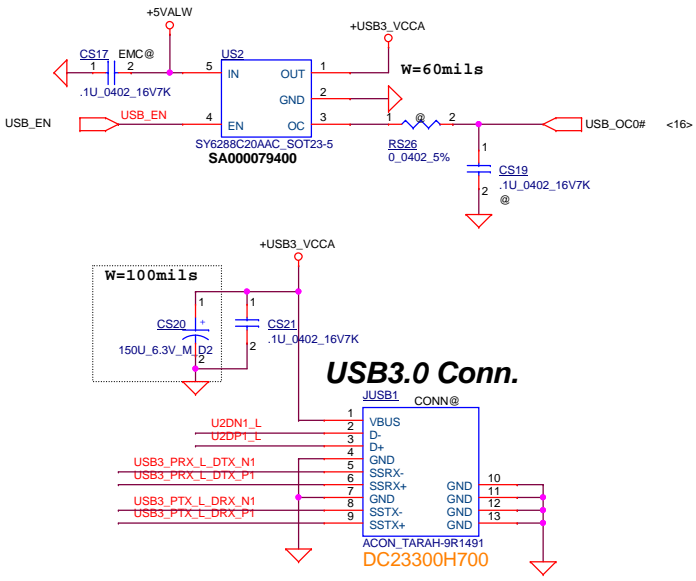
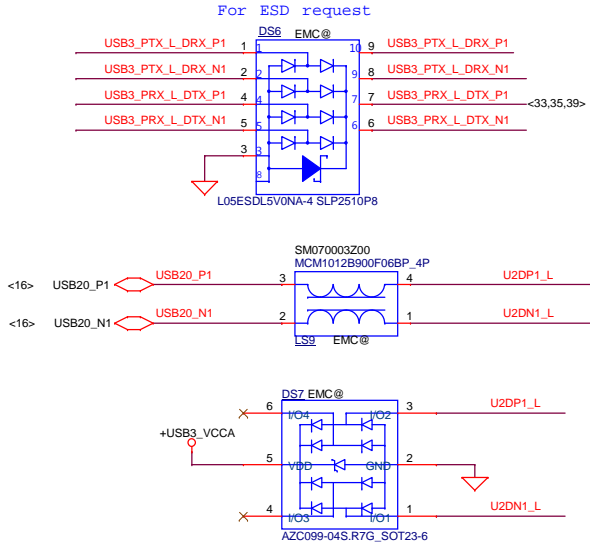
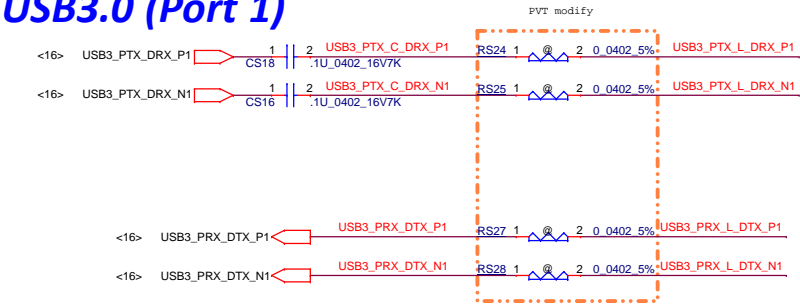


Table 3. USB Type-C Current Advertisement

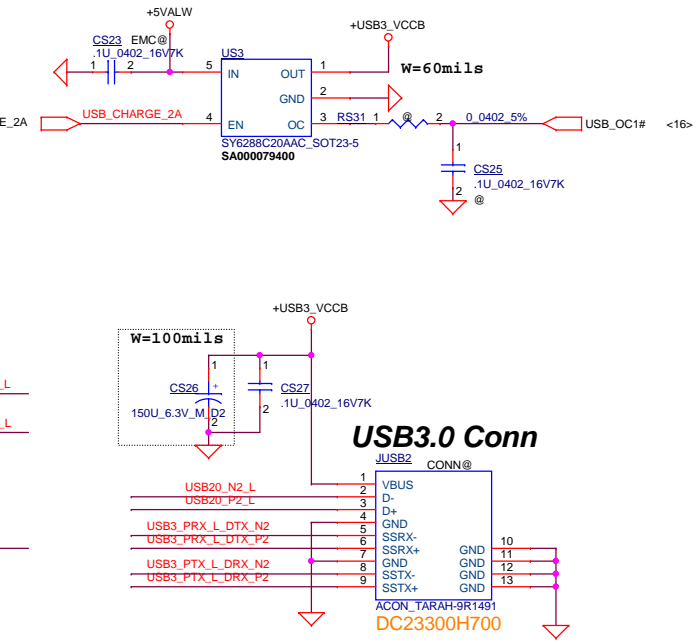
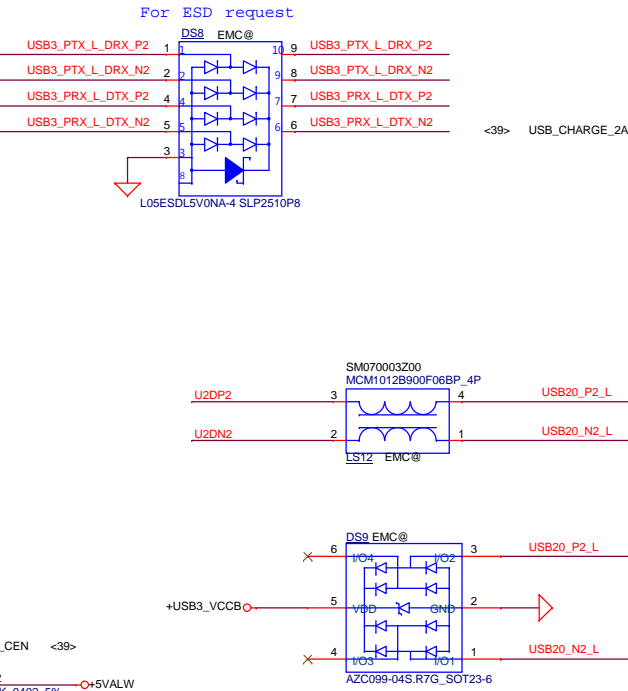
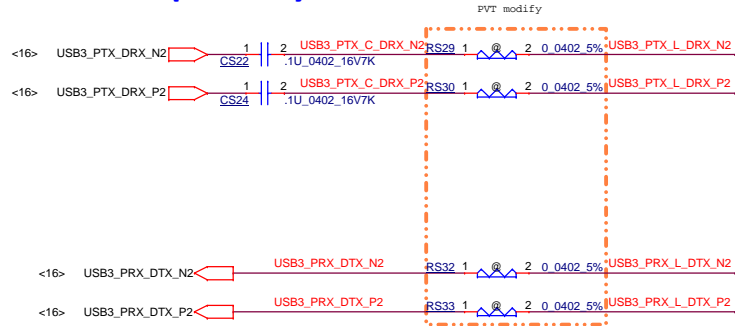
CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

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						Size	CC+USB TYPE C
						Document Number	C5PM2 M/BLA-E361P
						Date:	Friday, October 28, 2016
						Sheet	35 of 61

USB3.0 (Port 1)

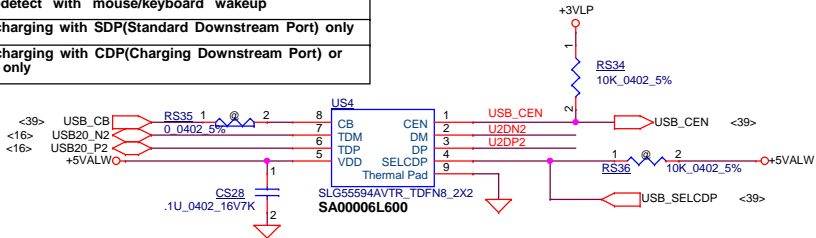


USB3.0 (Port 2)



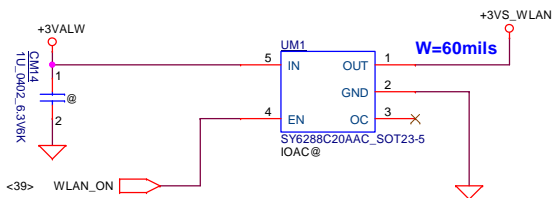
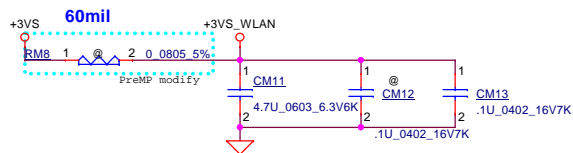
USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only



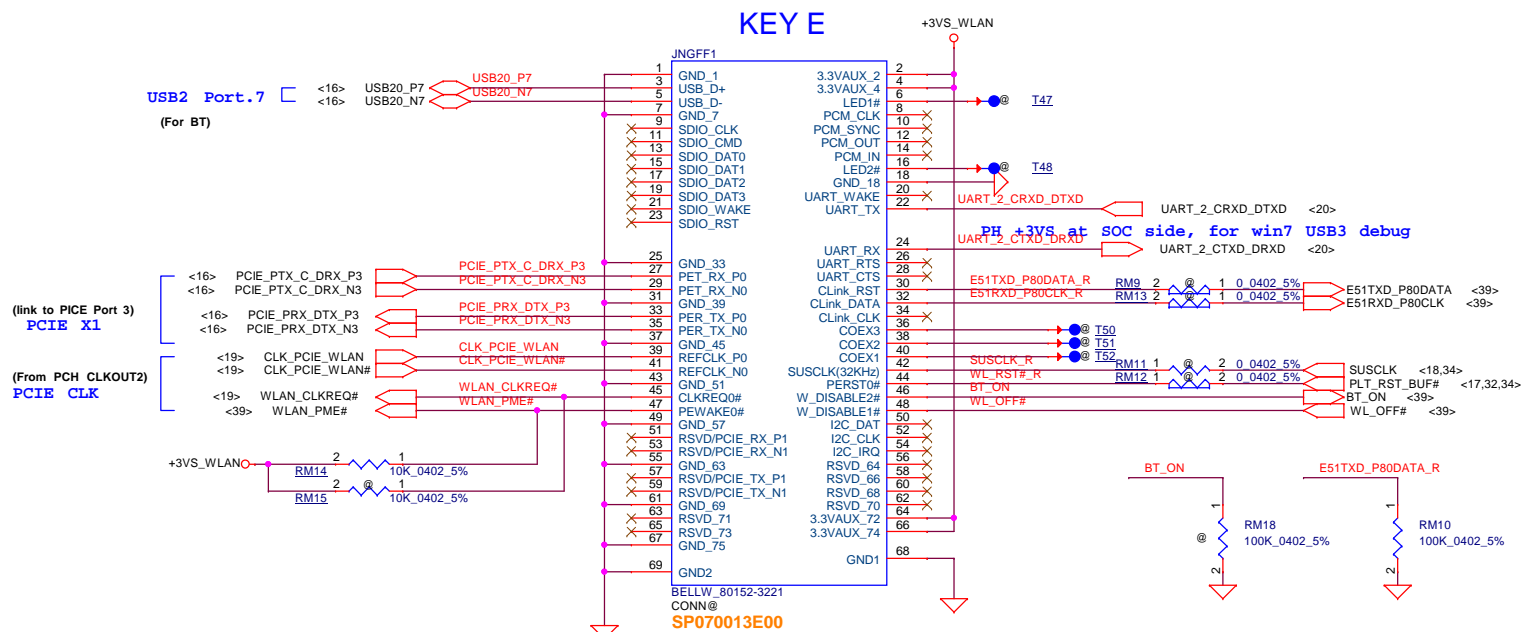


# Wireless LAN



## NGFF WL+BT (KEY E)

74	2.0V	GND	75
72	3.3V	RESERVED/REFCLKN1	73
70	UM_Power_SRC(GPIO/PEWake1#)	RESERVED/REFCLKP1	71
68	UM_Power_SINK(CLKREQ1#)	GND	69
66	UM_SWVP/PERST1#	Reserved/PERn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERT# (IO/3.3)	GND	63
60	DC CLK (IO/3.3)	Reserved/PERnL	61
58	DC DATA (IO/3.3)	Reserved/PERpL	59
56	W_DISABLEL1 (IO/3.3V)	GND	57
54	Reserved_W_DISABLE2 (IO/3.3V)	PEWakeDr (IO/3.3V)	55
52	PERST0# (IO/3.3V)	CLKREQ0# (IO/3.3V)	53
50	SUSCLK(32KHz) (IO/3.3V)	GND	51
48	CODE1 (IO/3.3V)	REFCLKN0	49
46	CODE2 (IO/3.3V)	REFCLKP0	47
44	CODE3 (IO/3.3V)	GND	45
42	VENDOR_DEFINED	PERn0	43
40	VENDOR_DEFINED	PERp0	41
38	VENDOR_DEFINED	GND	39
36	UART_RTS (IO/3.3V)	PERn0	37
34	UART_CTS (IO/3.3V)	PERp0	35
32	UART_TX (IO/3.3V)	GND	33
22	UART Rx (IO/3.3V)	SDIO Reset# (IO/3.3V)	23
20	UART Wake# (IO/3.3V)	SDIO Wake# (IO/3.3V)	21
18	GND	SDIO DAT3 (IO/3.3V)	19
16	LED#1 (V/CO)	SDIO DAT2 (IO/3.3V)	17
14	PCM_OUT/IS_SD_OUT (IO/3.3V)	SDIO DAT1 (IO/3.3V)	15
12	PCM_IN/IS_SD_IN (IO/3.3V)	SDIO DAT0 (IO/3.3V)	13
10	PCM_SYNC/IS_WS (IO/3.3V)	SDIO CMD (IO/3.3V)	11
8	PCM_CLK/IS_SCK (IO/3.3V)	SDIO CLK (IO/3.3V)	9
6	LED#1 (V/CO)	GND	7
4	3.3V	USB_D+	5
2	3.3V	USB_D-	3
1	GND	GND	1



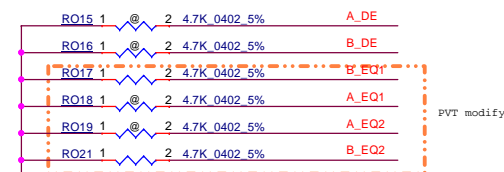
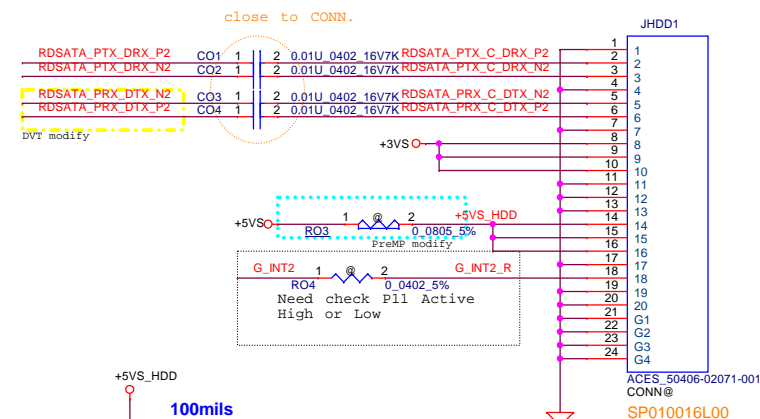
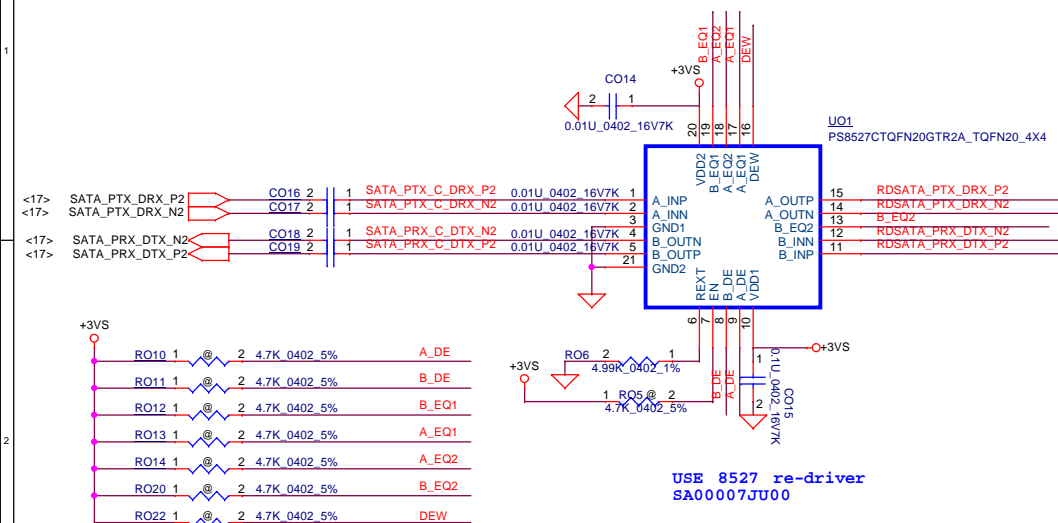
### 3.4-8.4-3.1.7.1. UART Wakeup

The UART power management protocol supports the following 4-wire and 5-wire interfaces:

- ☐ ~~RDN~~ **UART\_RXD** (Input): Receive Data
- ☐ ~~RTN~~ **UART\_TXD** (Output): Transmit Data
- ☐ **UART\_RTS** (Input): Request to Send (Host Flow Control)
- ☐ **UART\_CTS** (Output): Clear to Send (Device Flow Control)
- ☐ ~~Host Wake-Up~~ **UART\_Wake#** (Output): Host wake-up line is optional in case the host support in-band wake-up

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Date:	Friday, October 28, 2016	Sheet	37	of	61	

## SATA Re-Driver and cable HDD Conn.



Chip Enable, Internally pulled up at ~150K $\Omega$

EN	Status
L	Chip disabled
H	Chip enabled(default)

Programmable output de-emphasis level setting for channel A.  
Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.  
Internally tied to VDD/2(M status).

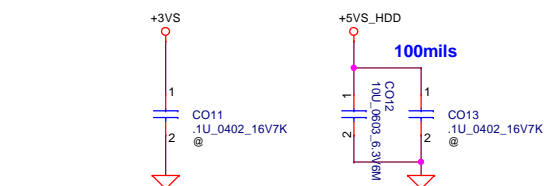
B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Equalizer control and program for channel A.  
Internally tied to VDD/2 (M status).

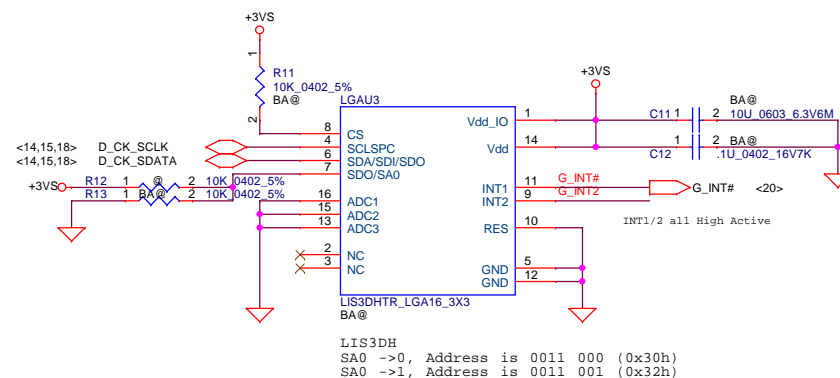
A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Equalizer control and program for channel B.  
Internally tied to VDD/2(M status).

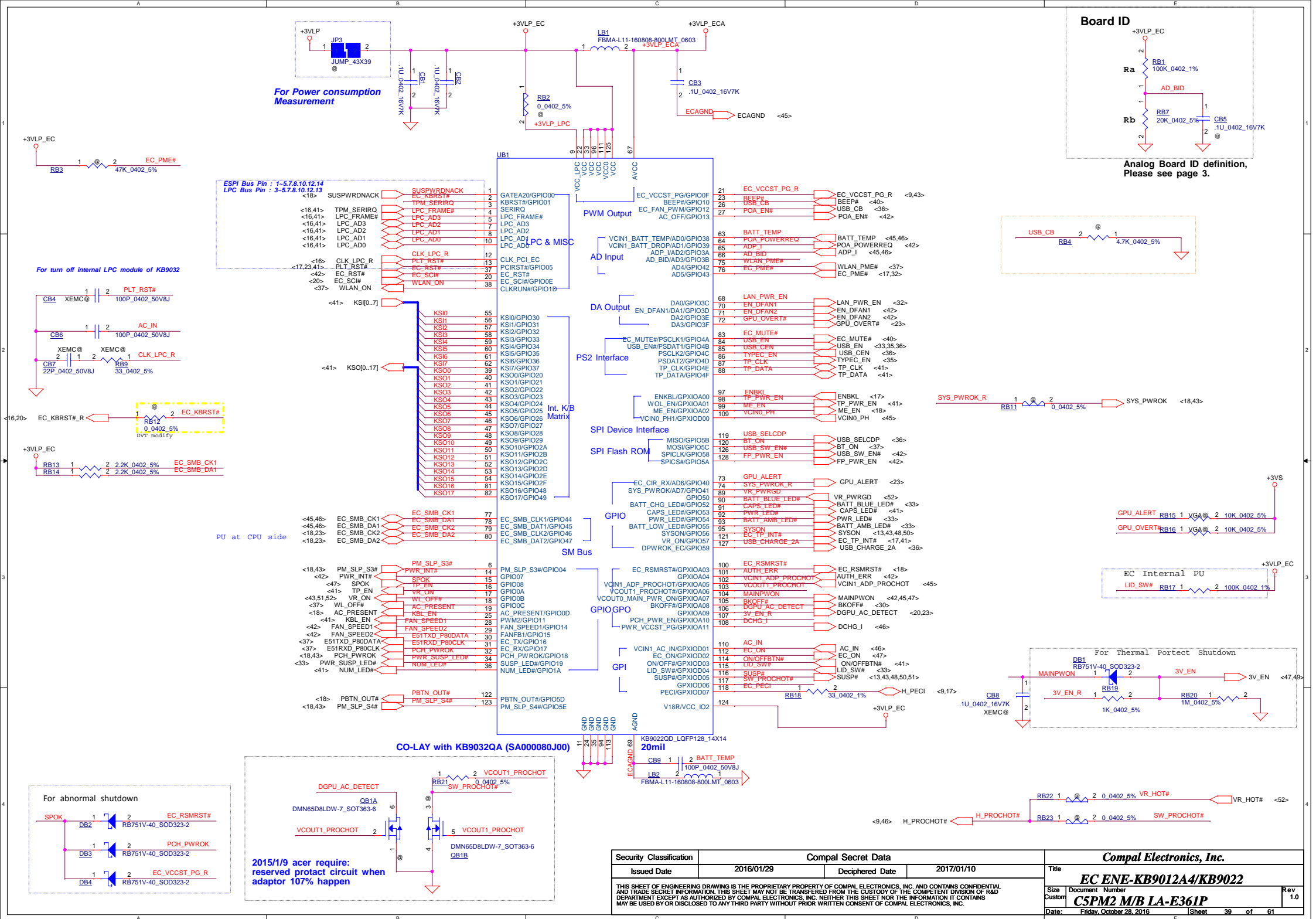
B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB



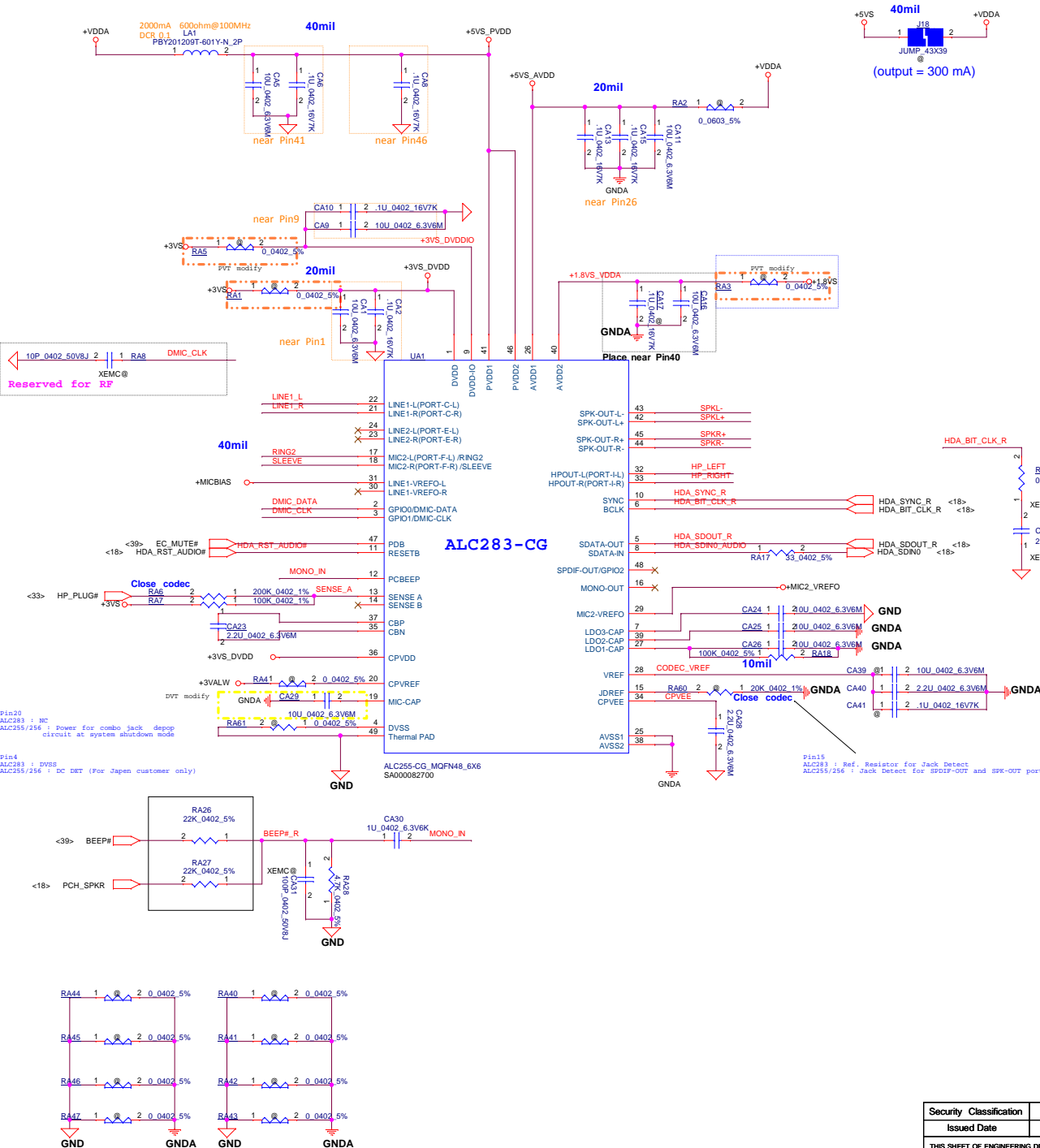
**G-Sensor reserved for BA serial**



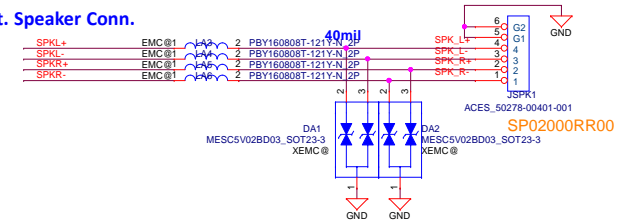
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				Size	Document Number	Rev
				C5PM2 M/B LA-E361P		
Date: Friday, October 28, 2016				Sheet	38	of 61



# HD Audio Codec

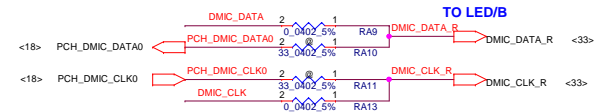


## Int. Speaker Conn.

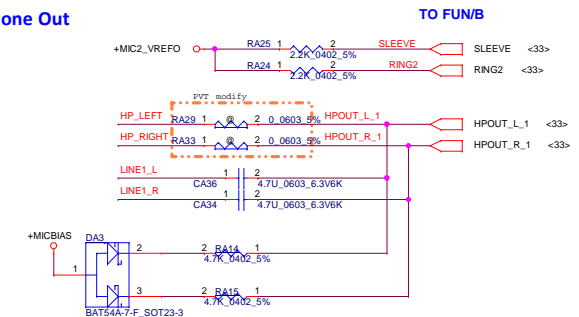


## Digital MIC

MIC BOM upload by Audio Team



## Headphone Out



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ON/OFFBTN#

ON/OFFBTN#

Test Only

BOT

SW1

EVOPLDA15 4P

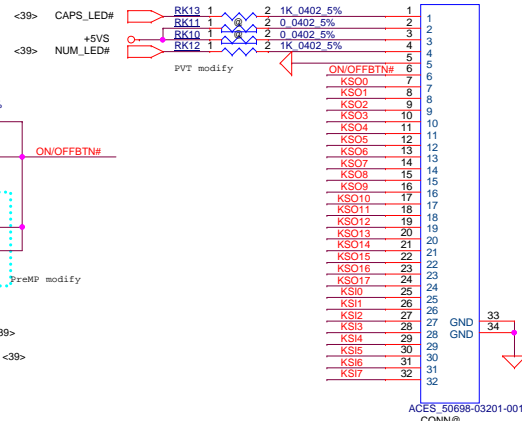
PreMP modify

KSIO[0..7]

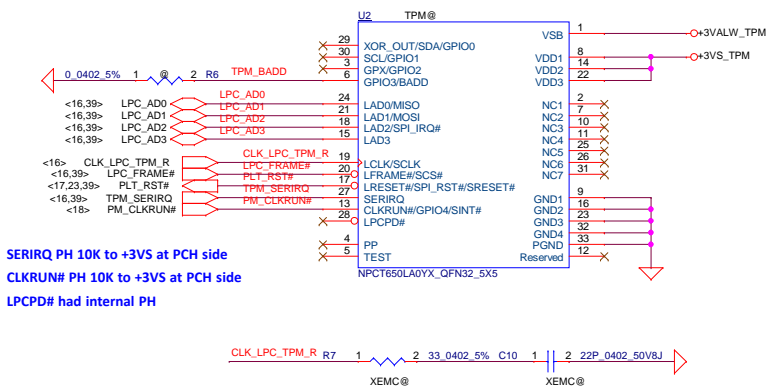
KSIO[0..7] <39>

KSO[0..17]

KSO[0..17] <39>



<b>BADD</b>	<b>SELECTION</b>
* 1	AEh(write), AFh(read)

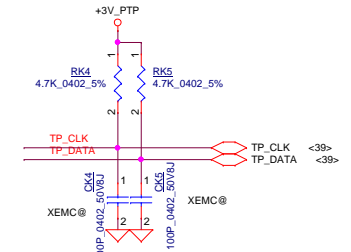
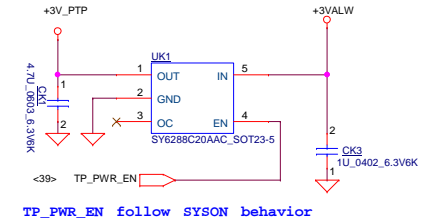
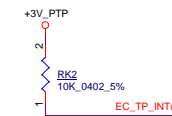
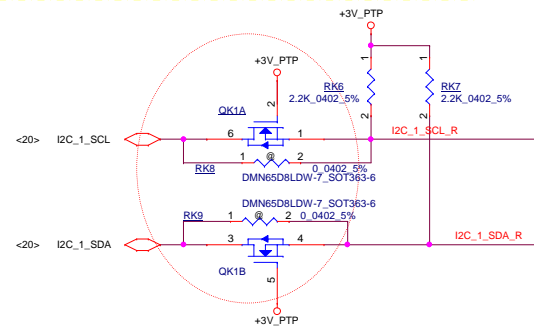


ACES\_51524-00801-001  
CONN@  
SP01001A910

1 TP\_CLK  
2 TP\_DATA  
3 I2C\_1\_SDA\_R  
4 I2C\_1\_SCL\_R  
5 EC\_TP\_INT#  
6 TP\_EN  
7 GND  
8 GND  
9 JTP1  
10 JTP1

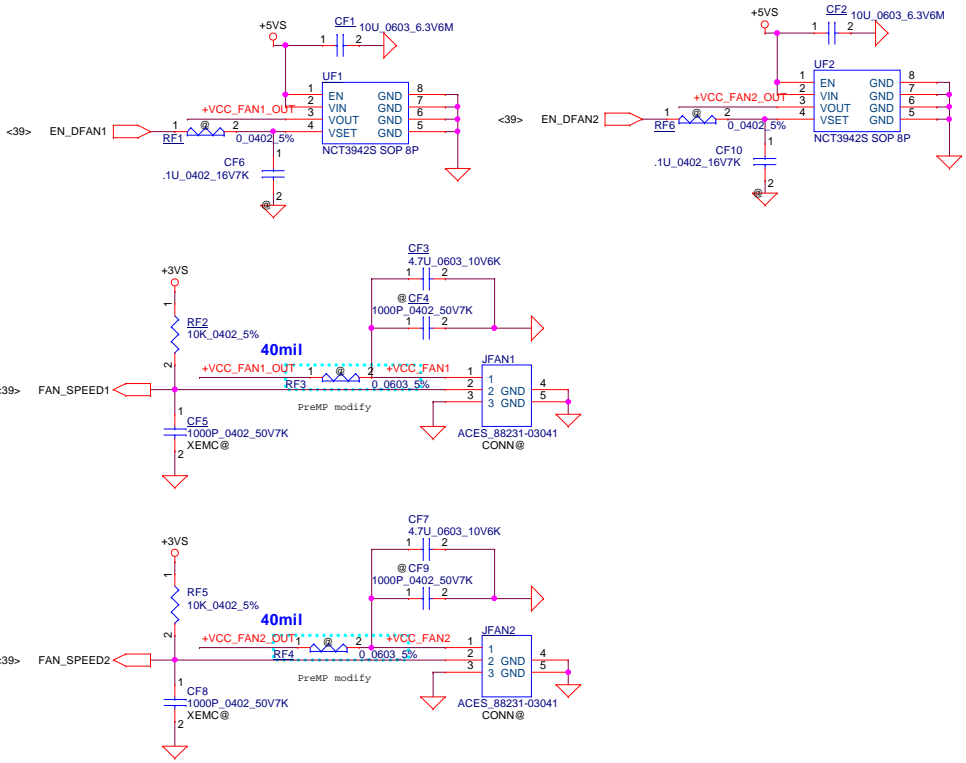
3V\_PTP  
3V\_ALV  
3V\_S  
CK2 @ .1U\_0402 16V7K  
EC PS2  
PCH I2C  
EC\_TP\_INT# <17,39>  
TP\_EN <39>

DVT modify



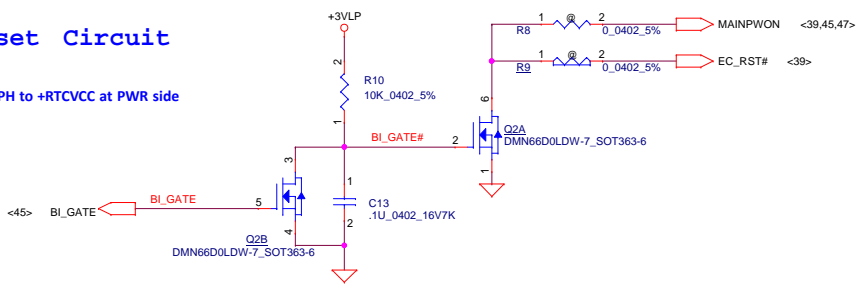


FAN Conn



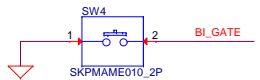
Reset Circuit

BI\_GATE PH to +RTCVC

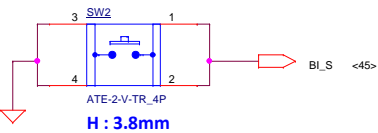


Reset But on

Reset But on

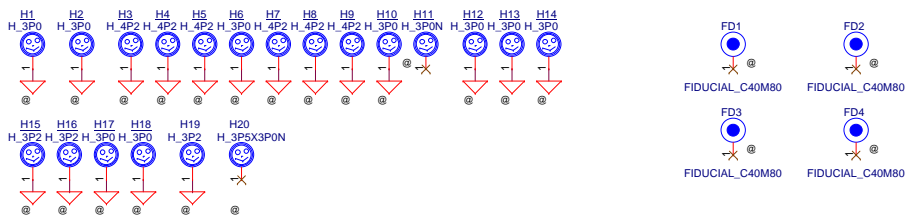


BI SW

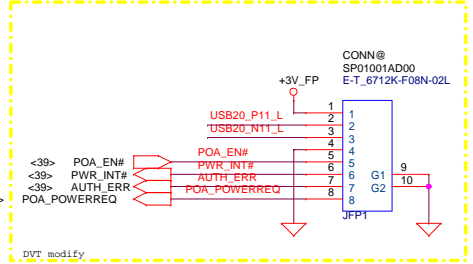
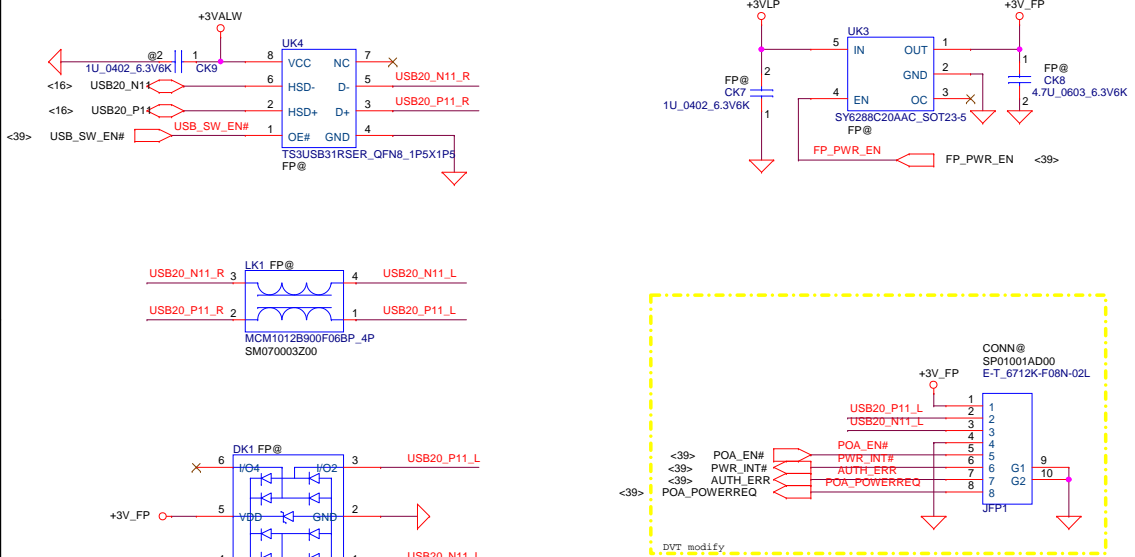


Release : Bat tery Of  
Push : Bat tery ON

Screw Hole



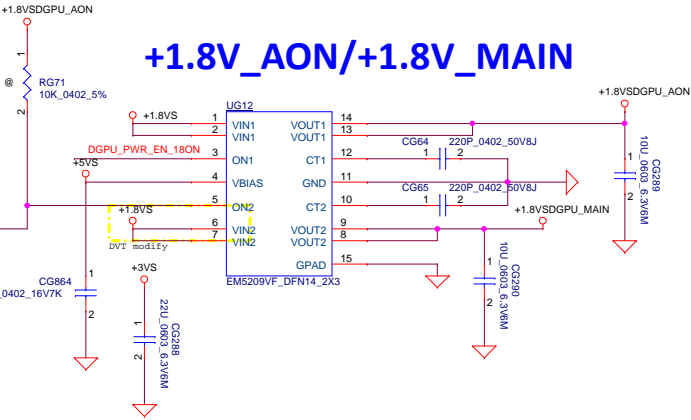
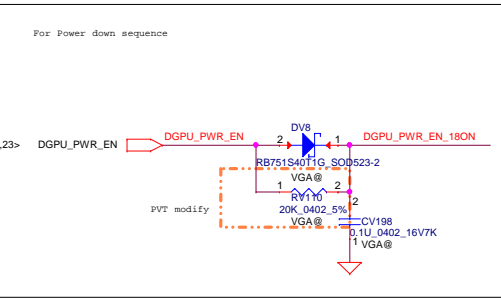
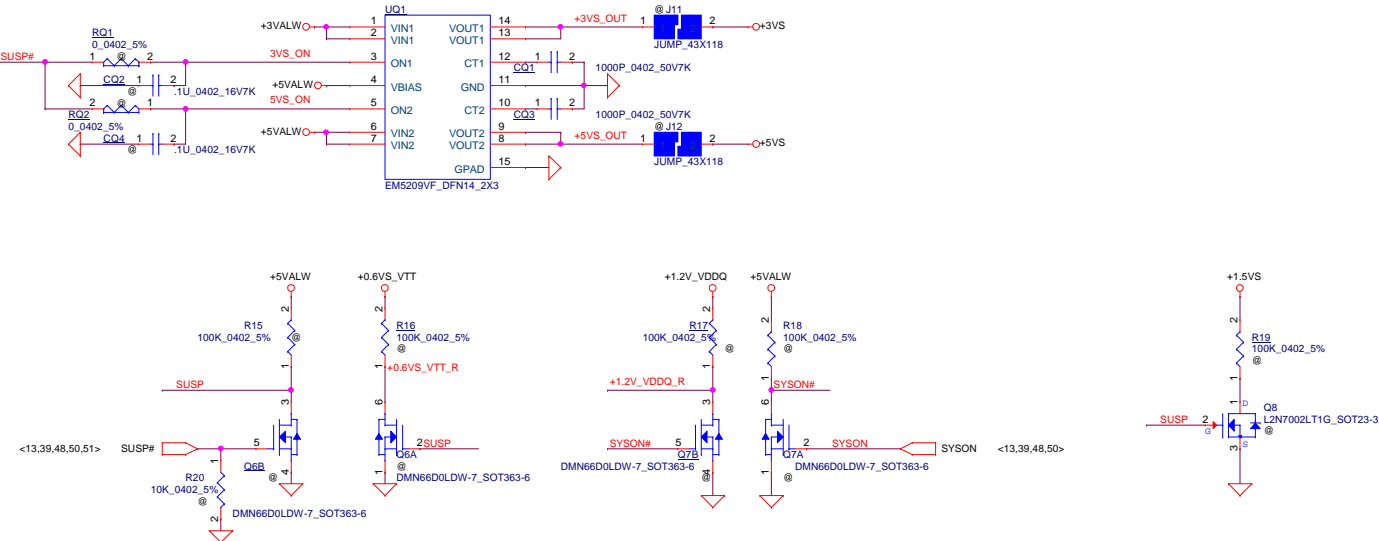
Finger Print POA



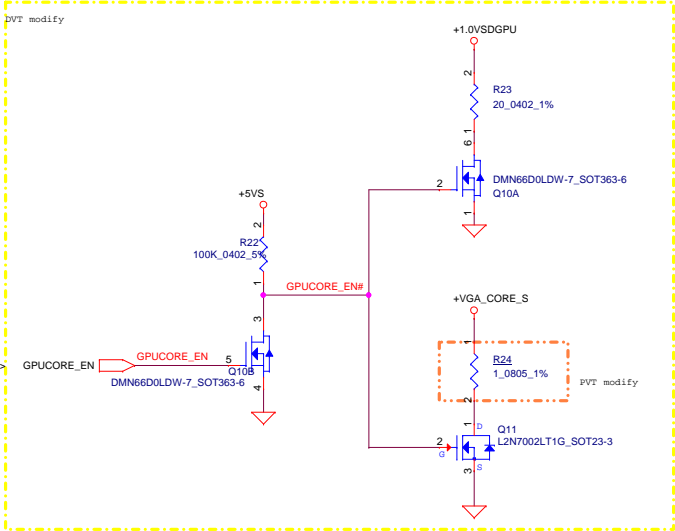
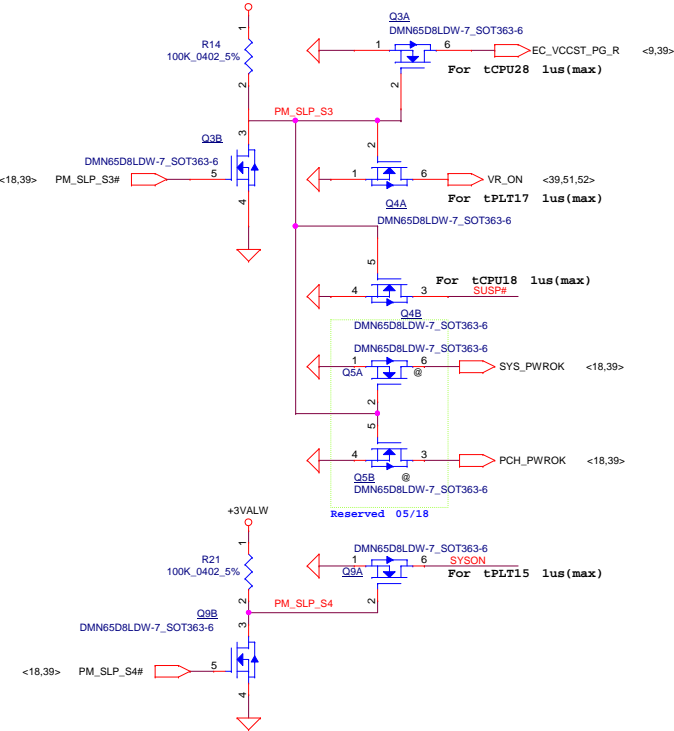
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Issued Date				2016/01/29		Deciphered Date		Title			
								FAN & FP & Screw Hole			
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								Date:		Friday, October 28, 2016	
								Sheet		42 of 61	
										Rev 1.0	

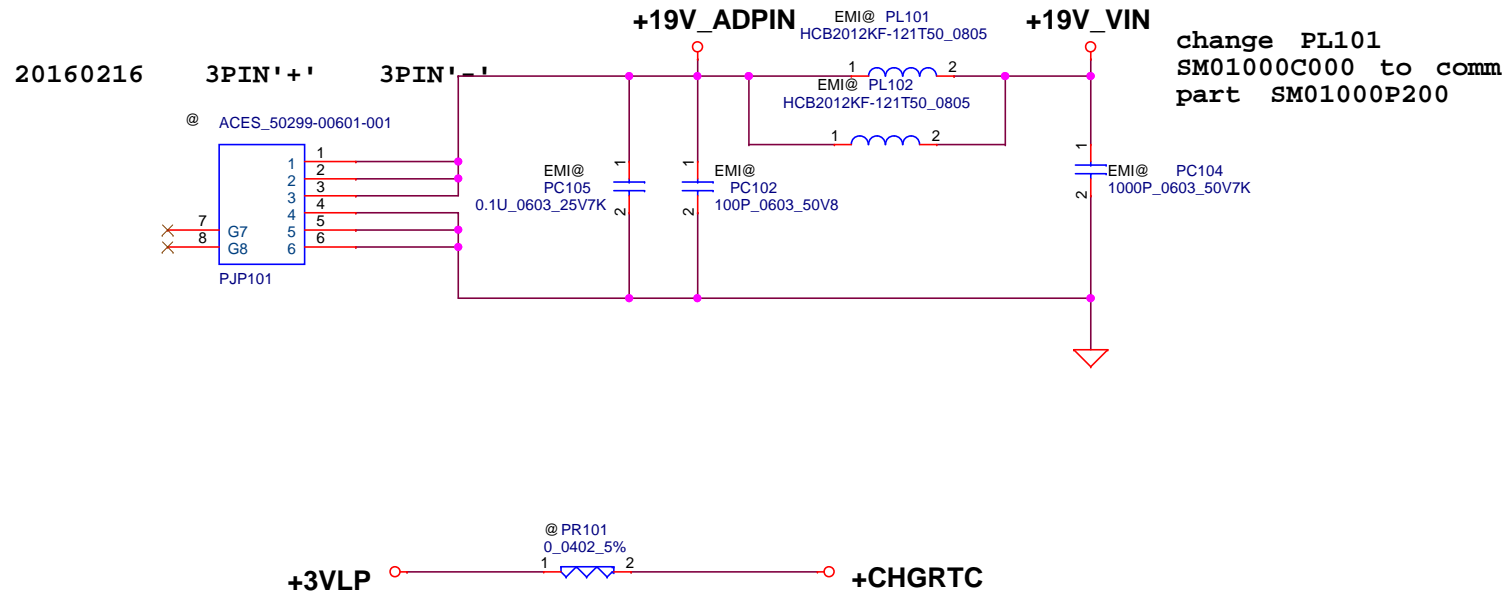


DC & VGA Interface



For Power Of f Sequence





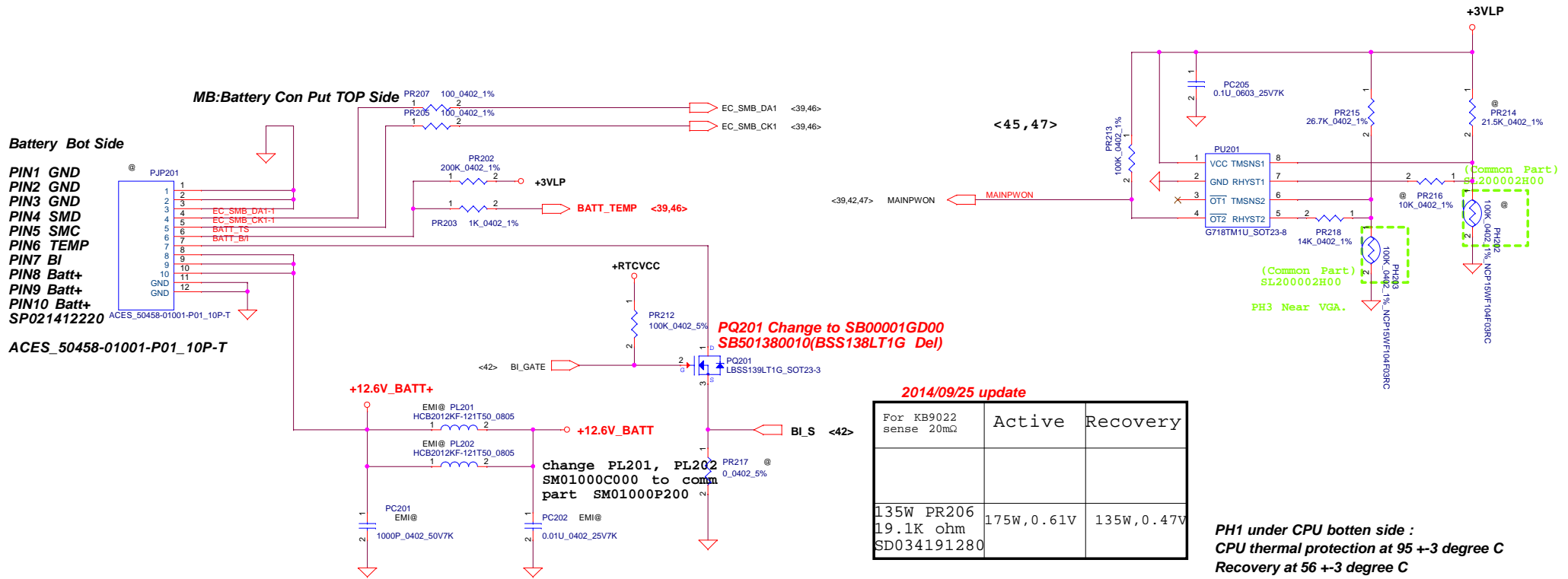
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				Date:	Friday, October 28, 2016	Sheet 44 of 61

# Battery Bot Side

PIN1 GND  
PIN2 GND  
PIN3 GND  
PIN4 SMD  
PIN5 SMC  
PIN6 TEMP  
PIN7 BI  
PIN8 Batt+  
PIN9 Batt+  
PIN10 Batt+  
SP021412220

ACES\_50458-01001-P01\_10P-T

## MB:Battery Con Put TOP Side

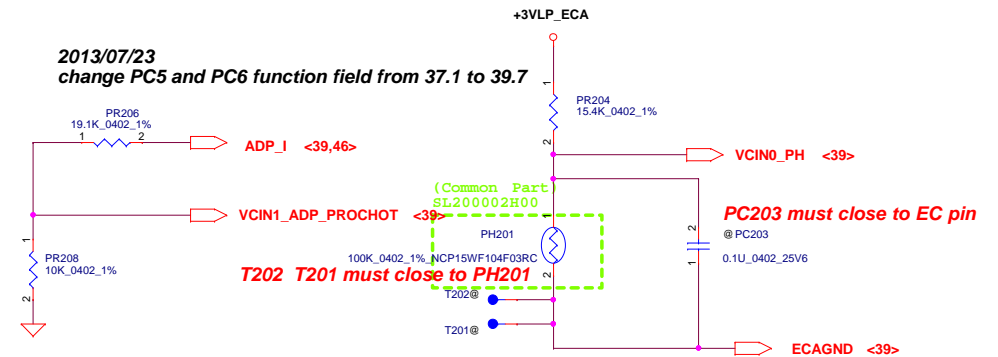


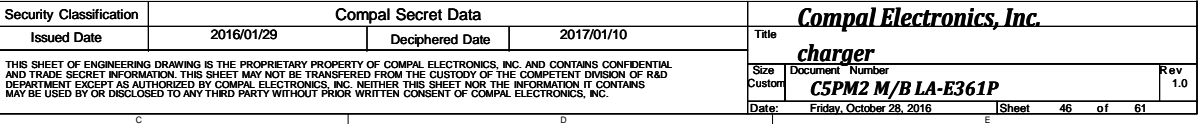
2014/09/25 update

For KB9022 sense 20mΩ	Active	Recovery
135W PR206 19.1K ohm SD034191280	175W, 0.61V	135W, 0.47V

PH1 under CPU botten side :  
CPU thermal protection at 95 +3 degree C  
Recovery at 56 +3 degree C

2013/07/23  
change PC5 and PC6 function field from 37.1 to 39.7



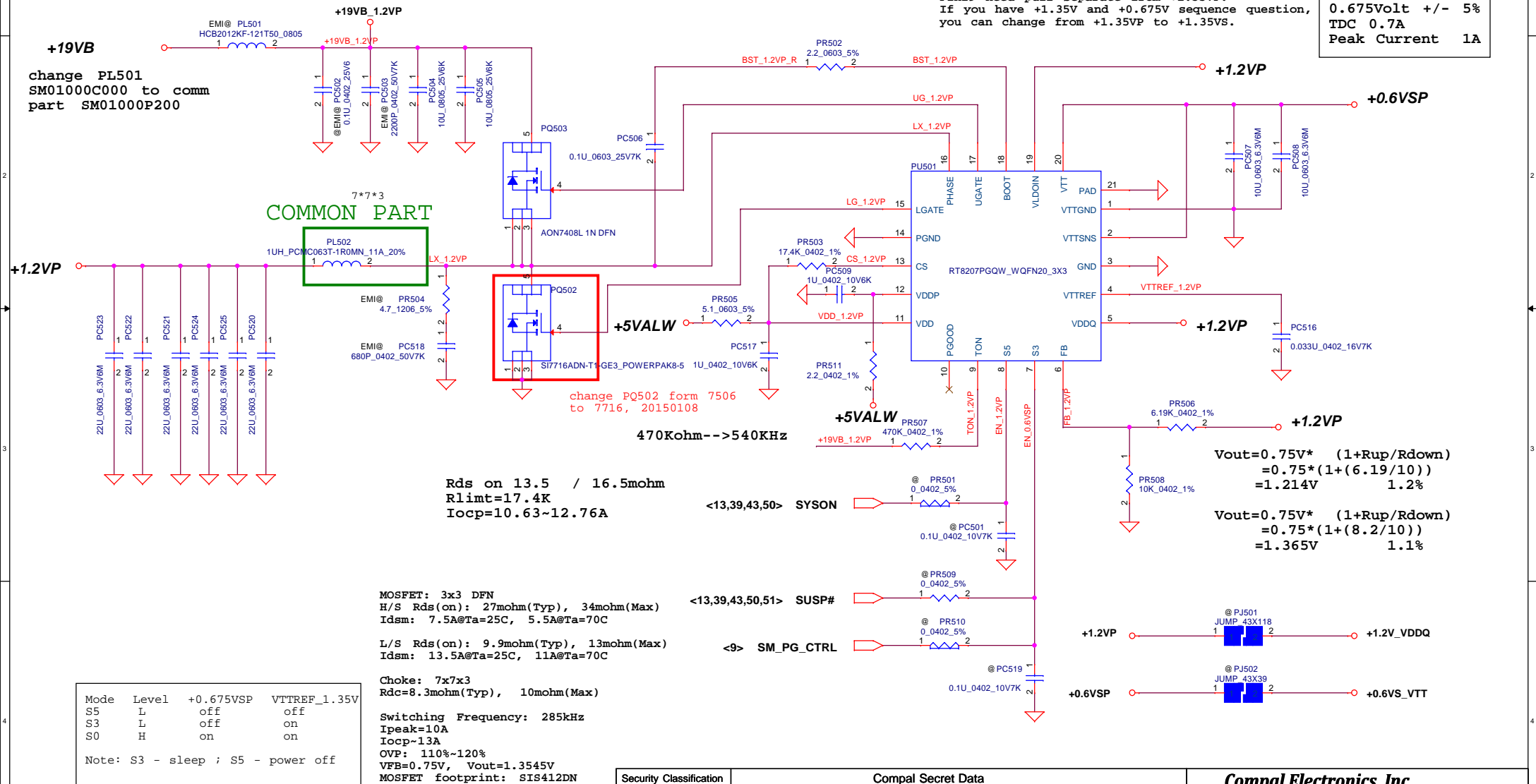




RT8207M_V1.mdd	For Single layer
RT8207M_V2.mdd	For Dual layer

RT8207M_V1.mdd	For Single layer
RT8207M_V2.mdd	For Dual layer

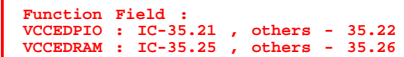
0.675Volt	+/-	5%
TDC	0.7A	
Peak Current	1A	



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				Custom	1.0
				<b>C5PM2 M/B LA-E361P</b> Date: Friday, October 28, 2016      Sheet 48 of 61	

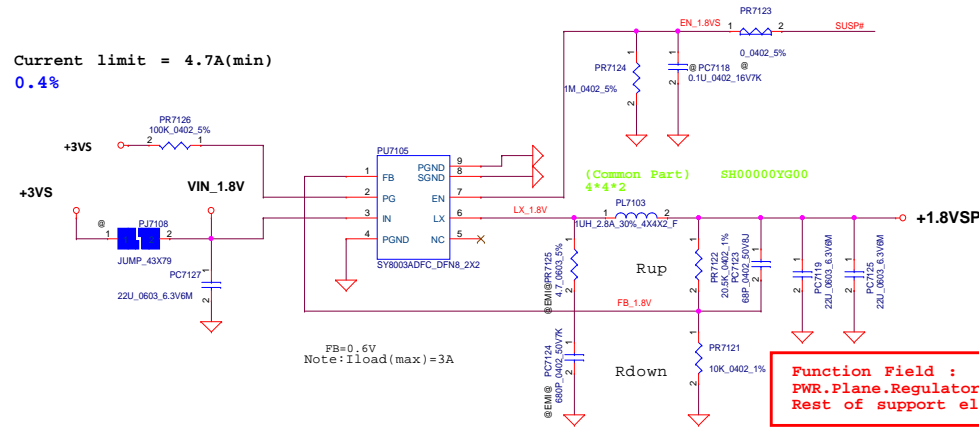


## SYX196D\_V3.mdd



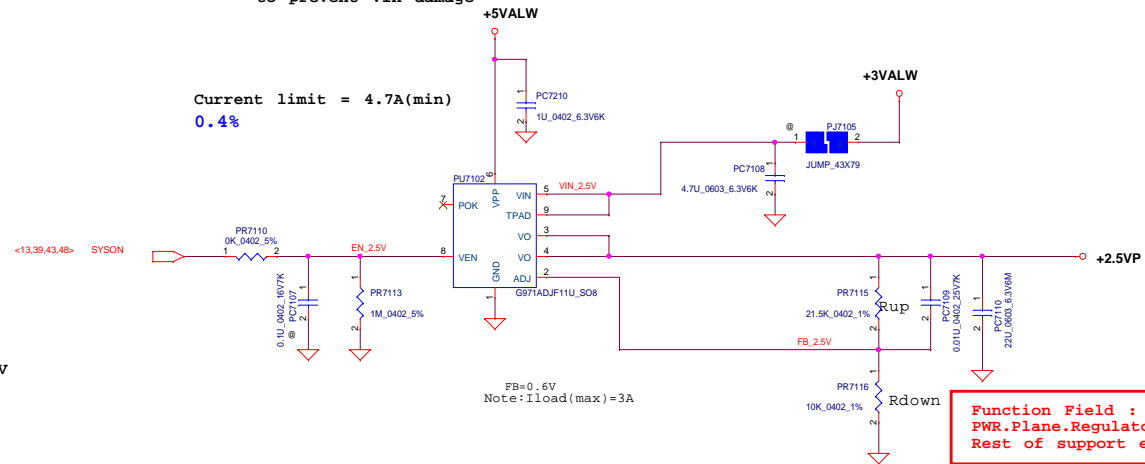
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					<b>CSPM2 M/B LA-E361P</b>	<b>1.0</b>
				Date:	Friday, October 28, 2016	Sheet 49 of 61

Current limit = 4.7A(min)  
0.4%



Note:  
When design Vin=5V, please stuff snubber  
to prevent Vin damage

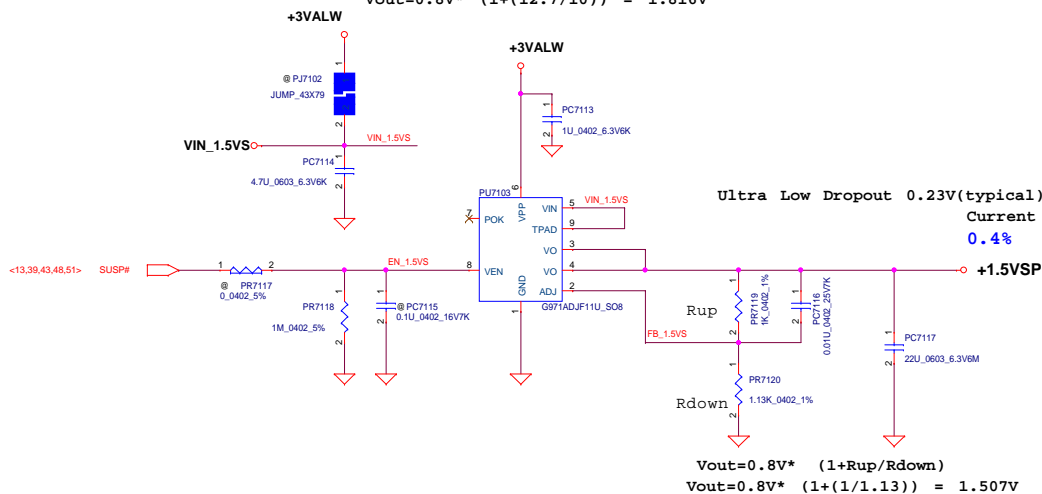
Current limit = 4.7A(min)  
0.4%



$$V_{out}=0.8V * (1+(21.5/10)) = 2.52V \quad 0.8\%$$

$$V_{out}=0.8V * (1+(12.7/10)) = 1.816V$$

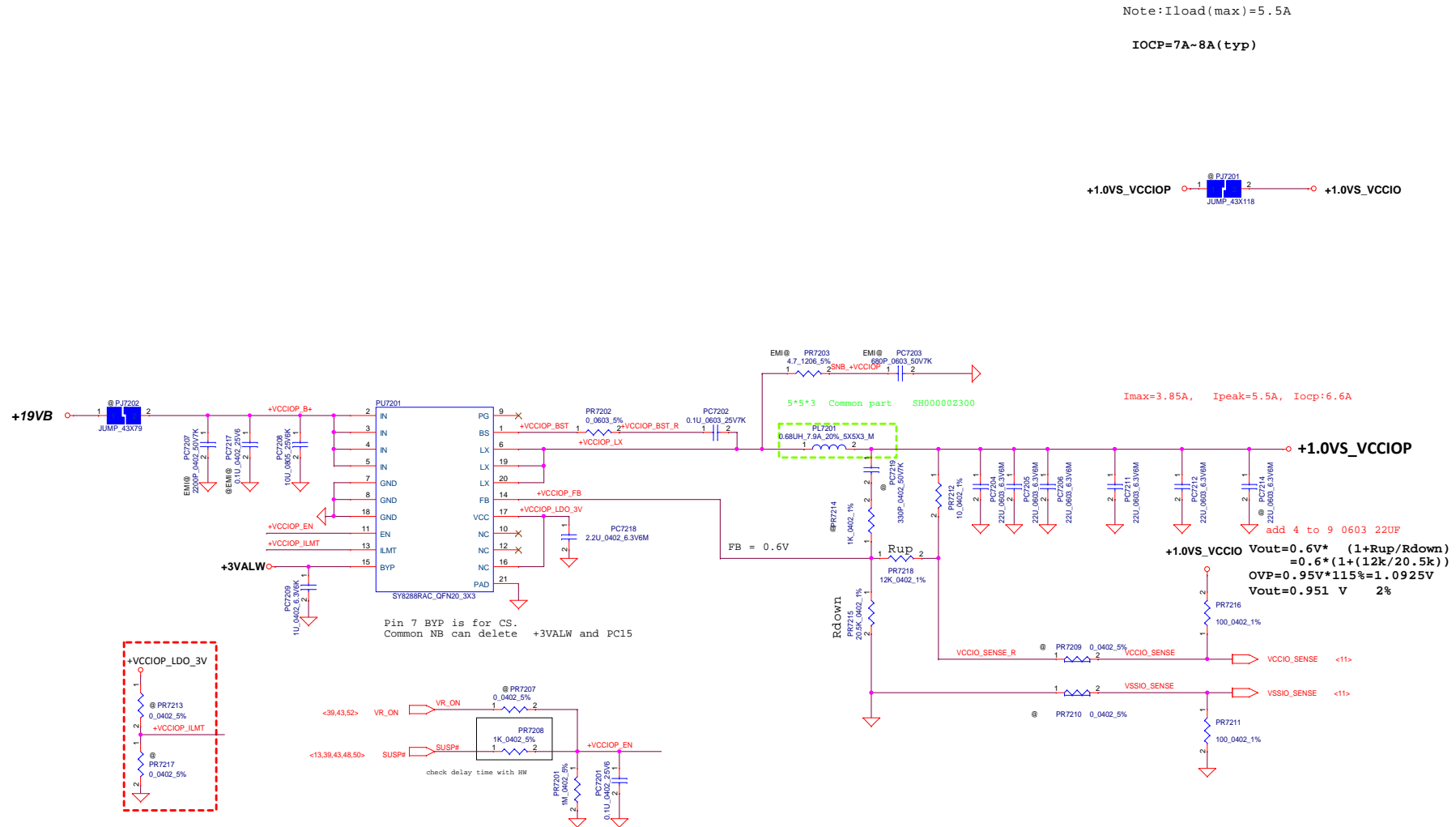
Ultra Low Dropout 0.23V(typical) at 3A Output Current  
Current limit = 4.7A(min)  
0.4%



$$V_{out}=0.8V * (1+(1.13/10)) = 1.507V$$

+1.5VSP:  
I<sub>max</sub>=0.5A I<sub>peak</sub>=0.75A

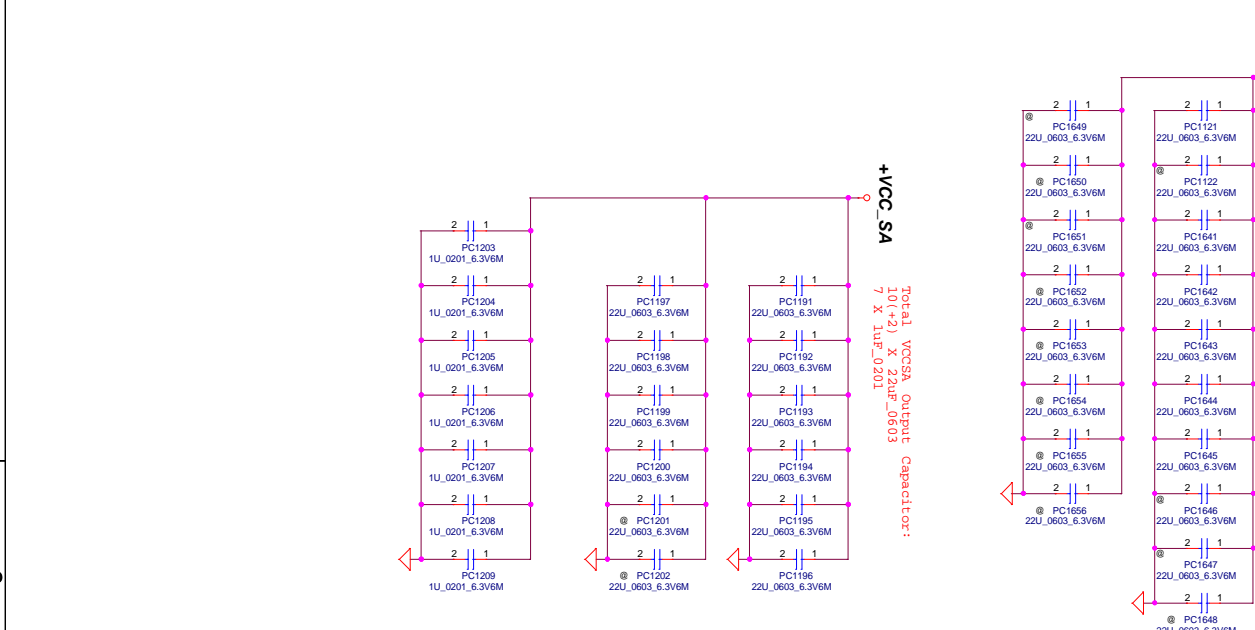
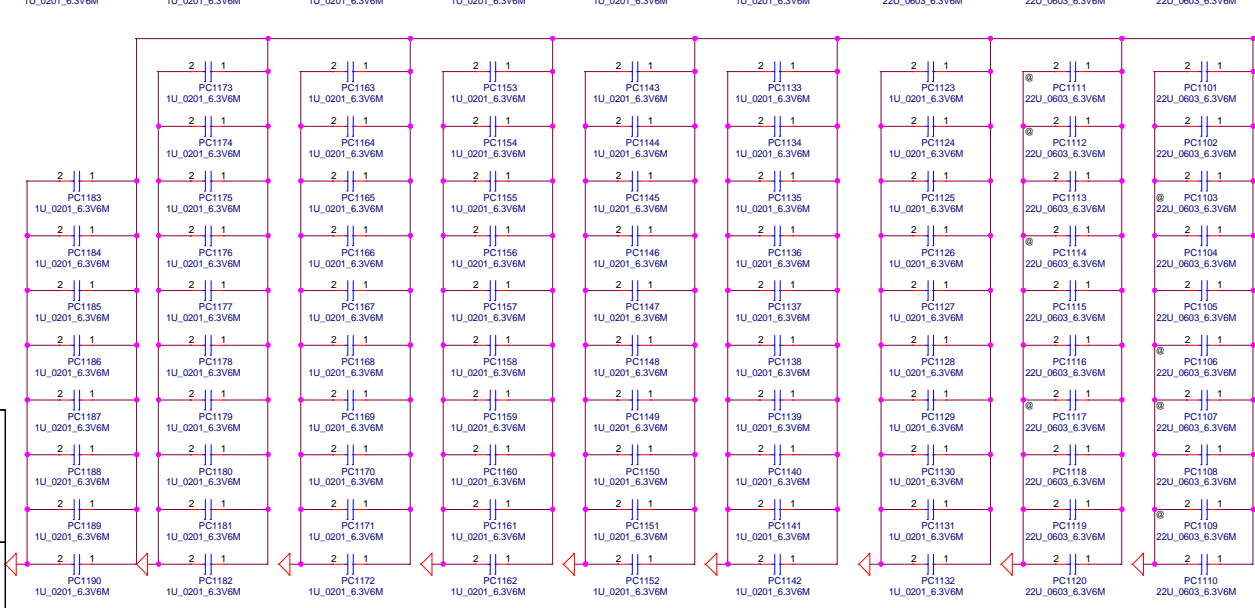
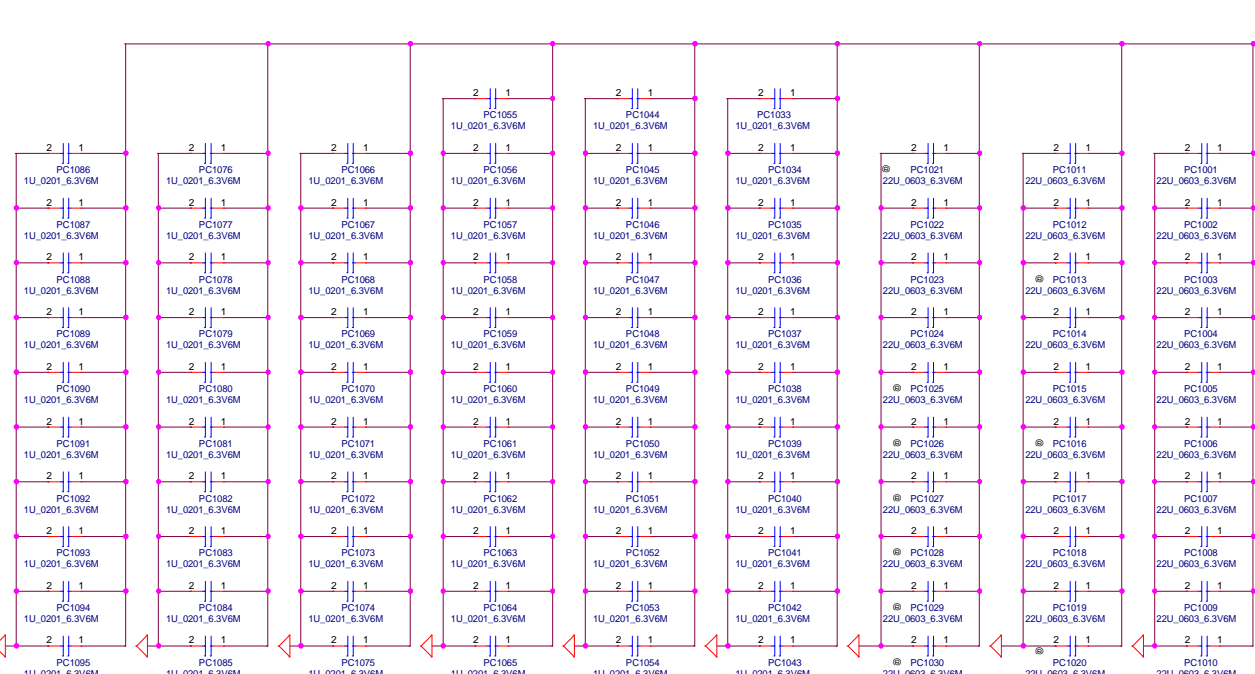
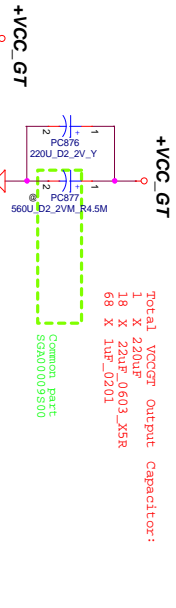
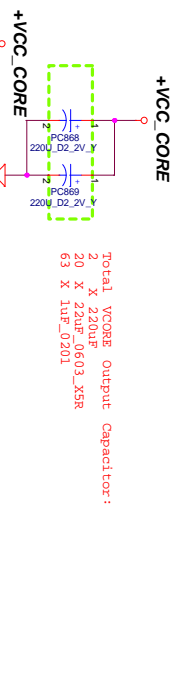
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Date:	Friday, October 28, 2016	Sheet	51	of 61





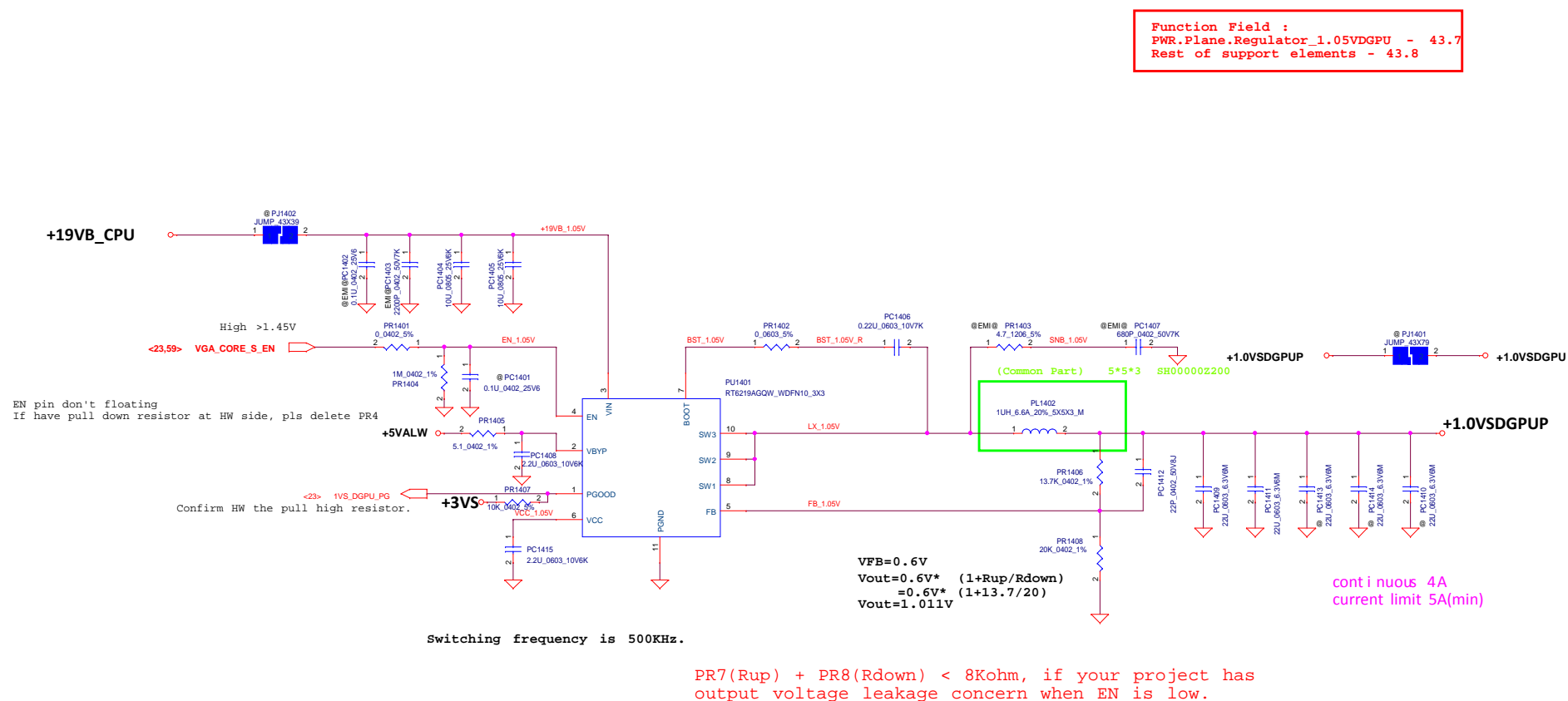


Security Classification				Compal Secret Data				Title			
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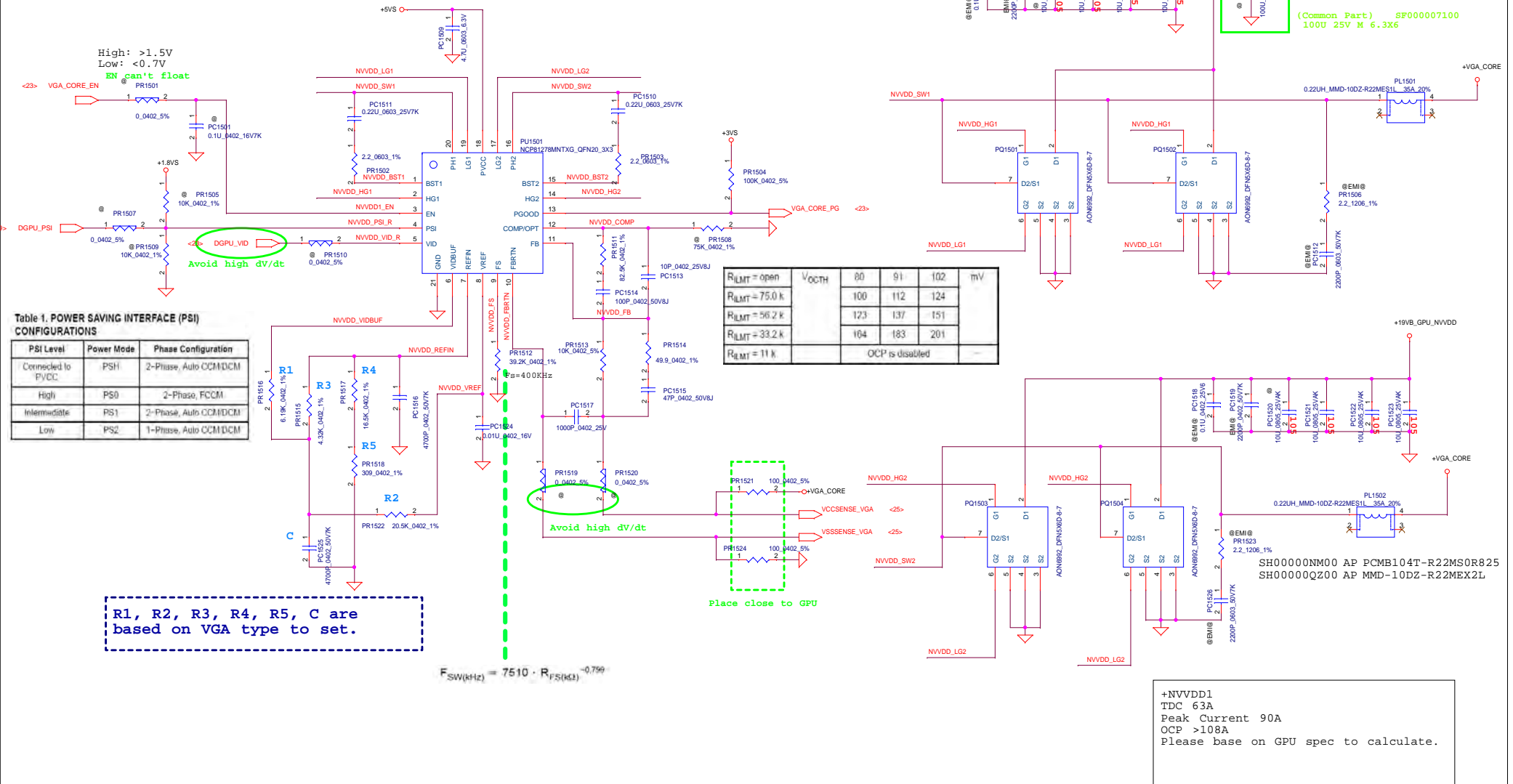




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				Rev	1.0

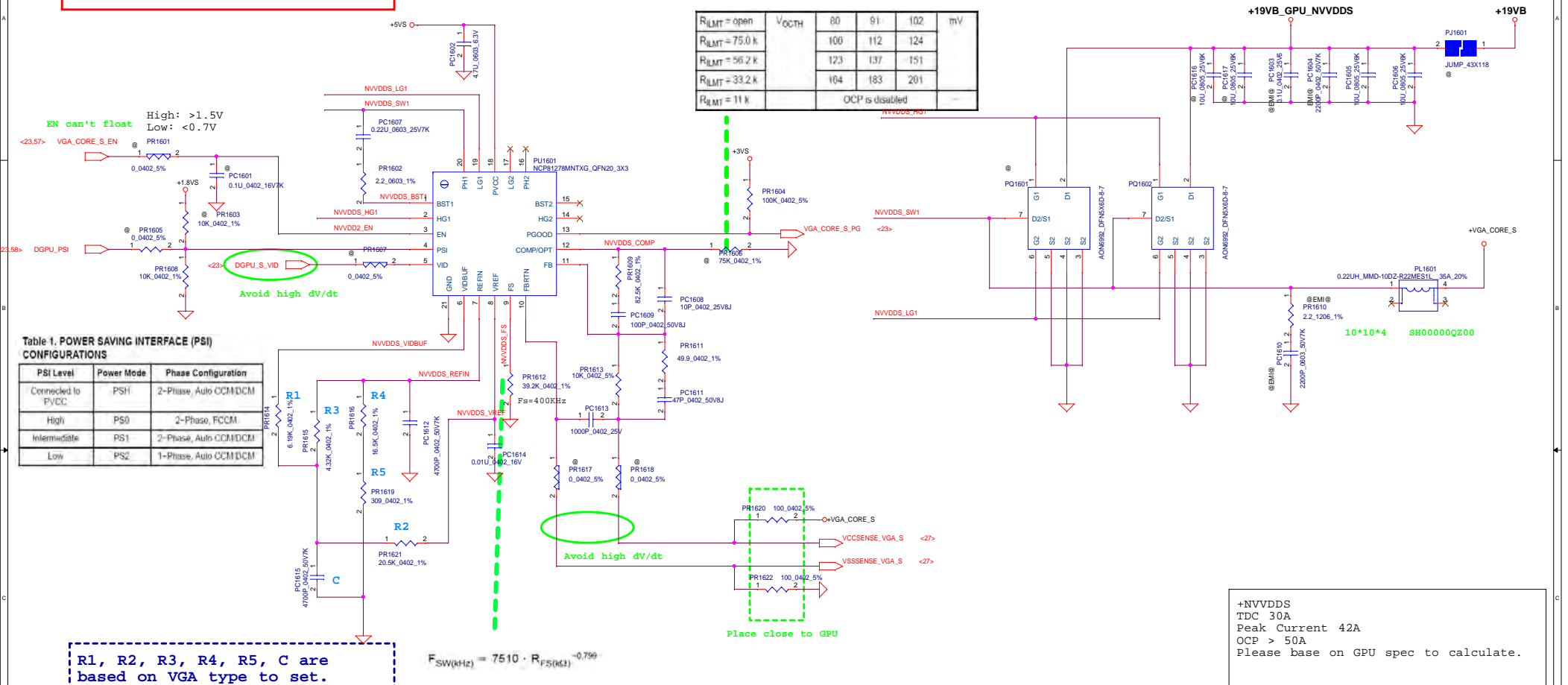
## Module model information

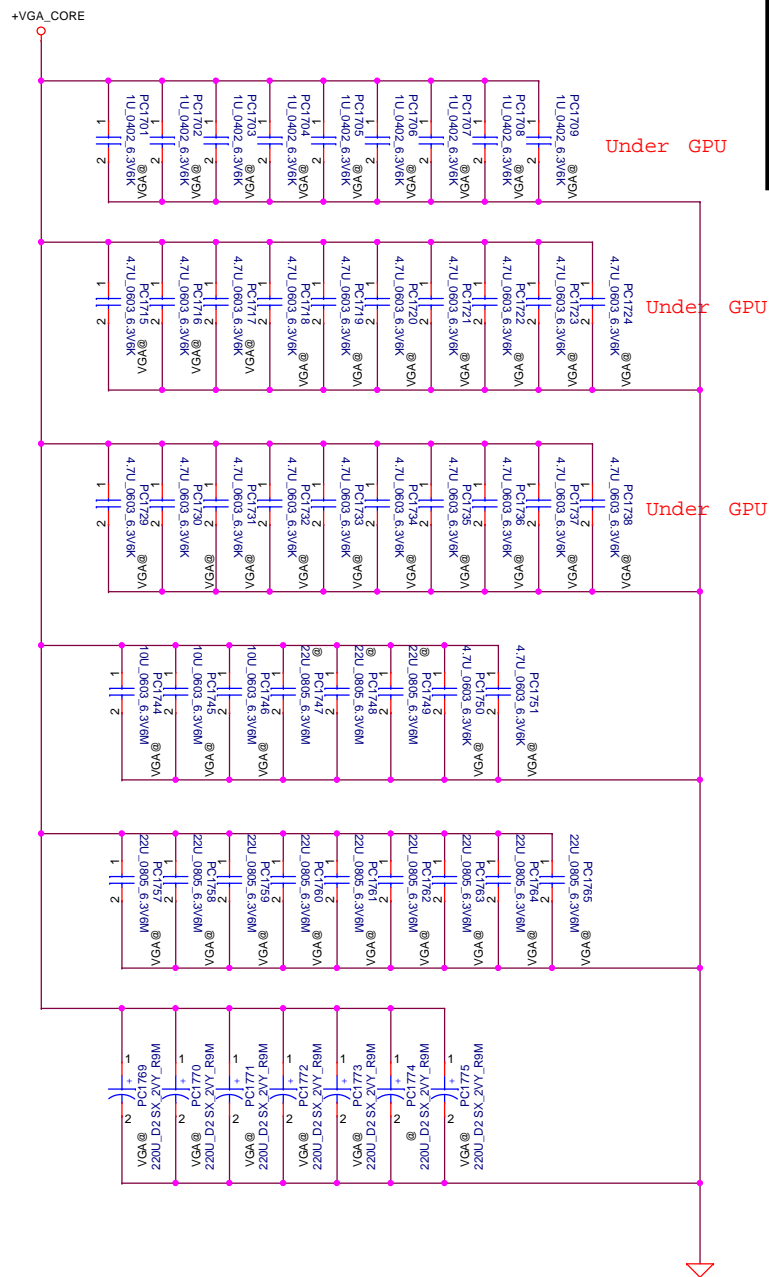
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NCP81278\_NVVDD\_V1B.mdd for SW portion.



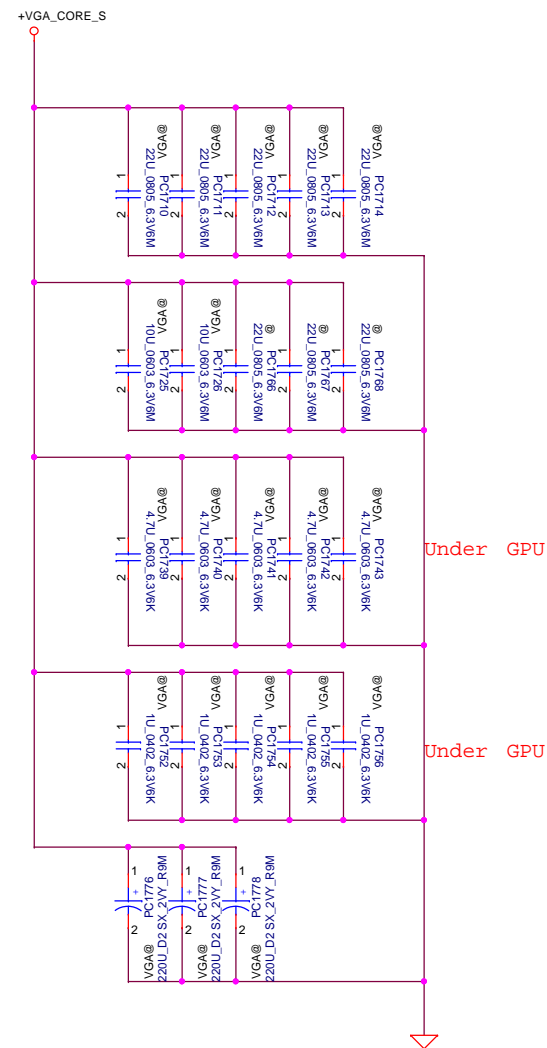
# Module model information

NCP81278\_NVVDDS\_V1A.mdd for IC portion.  
NCP81278\_NVVDDS\_V1B.mdd for SW portion.





+VGA_CORE	
470uF X 2	
330uFX2	
4.7uF_0603 X 22	
22uF_0603 X 7	
10uF_0603X 3	
1uF_0402 X 9	



```
+VGA_CORE_S
470uF X 2
22uF_0603_X5R X 3
10uF_0603 X 2
4.7uF_0603 X5
1uF_0402 X 5
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Page 1 of 1  
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